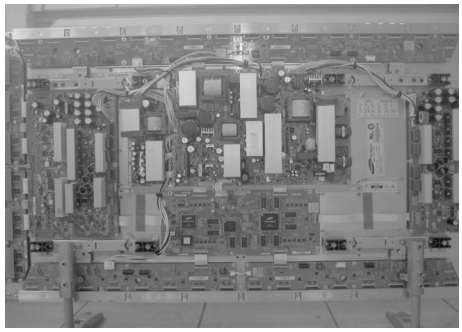
Service
Service
Service

LC 4.7, FM 242 (FTV2.1), FTP 1.1, FTP 2.2 X



Supplement SDI PDP Repair Manual

Service Manual

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PHILIPS

1. Technical Specifications

1.1 Model / Chassis overview

PDP Type	Model Name	H x V Pixel	Chassis
37”SDv4	S37SD-YD02 (*) S37SD-YB01	852 x 480	LC4.7
42”SDv2	S42SD-YD06 (*) S42SD-YB04	852 x 480	FM242 (FTV2.1) FTP1.1
42”SDv3	S42SD-YD05 (*) S42SD-YB03	852 x 480	LC4.7 FTP2.2x
42”HDv3	S42AX-XD03 (*) S42AX-XB01	1024 x 768	FTP2.2U
50HDv3	S50HW-XD03 (*) S50HW-XB02	1366 x 768	FTP2.2E

(*) are Model names with PSU, but only PDP model without PSU will be delivered as spare part

42" SDv2

External View

M3 = X Board + Y Board + Logic Board + PSU + SUB PSU

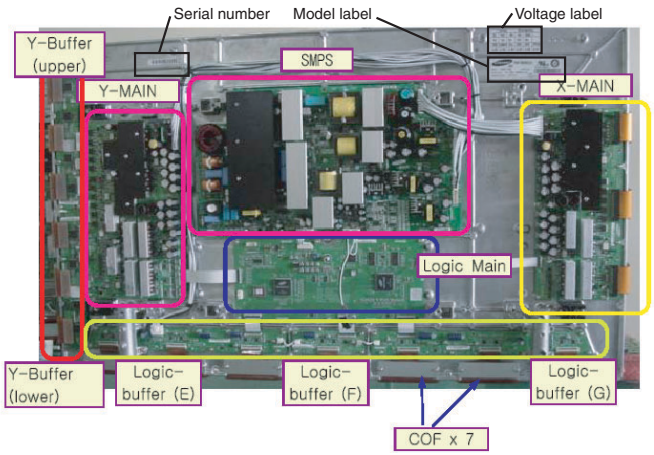


Figure 1-1

42" SDv3

External View

M3 = X Board + Y Board + Logic Board + PSU + SUB PSU

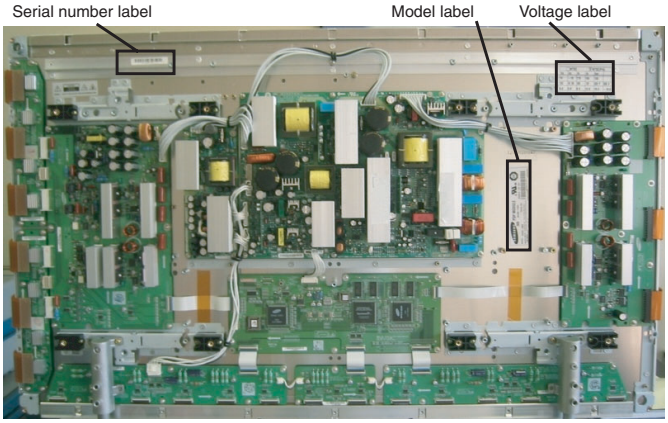


Figure 1-2

Points of Screw Mount

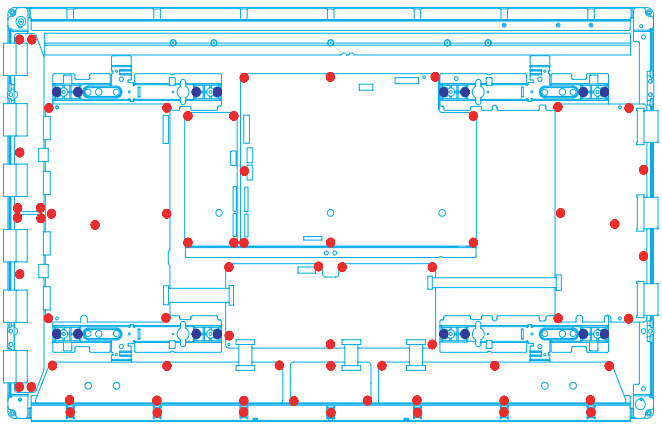


Figure 1-3

42"HDv3

External View
M3 = X Board + Y Board + Logic Board + PSU + SUB PSU

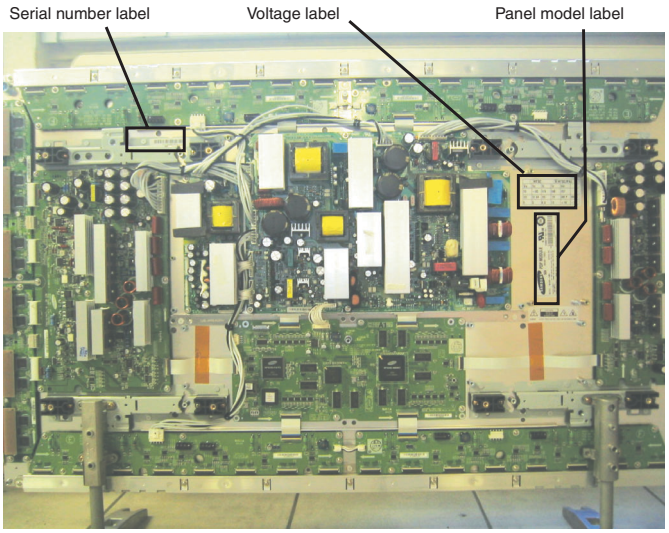


Figure 1-4

Points of Screw Mount

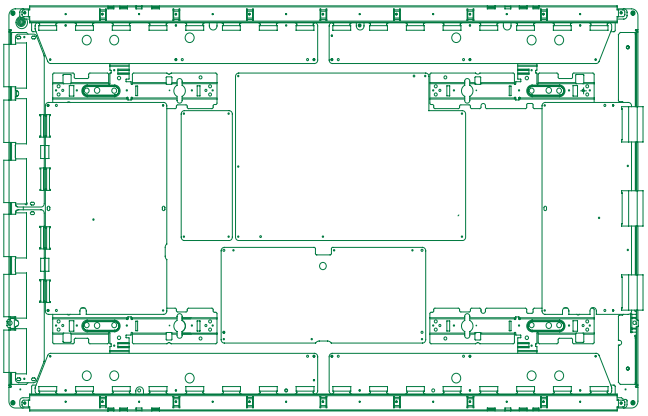


Figure 1-5

37" SDv4

External View
M3 = X Board + Y Board + Logic Board + PSU + SUB PSU ‘

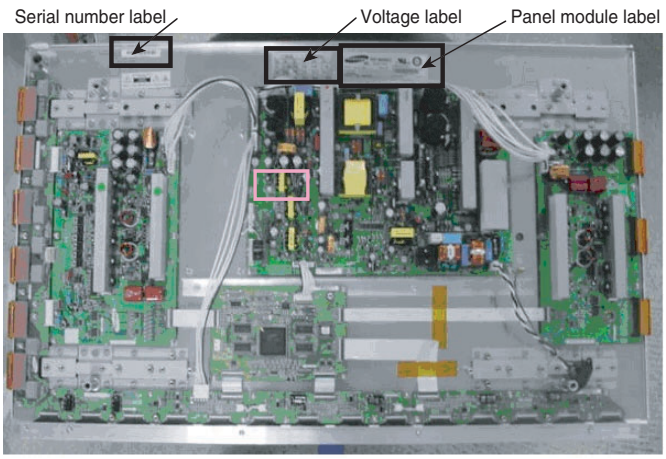


Figure 1-6

Points of Screw Mount

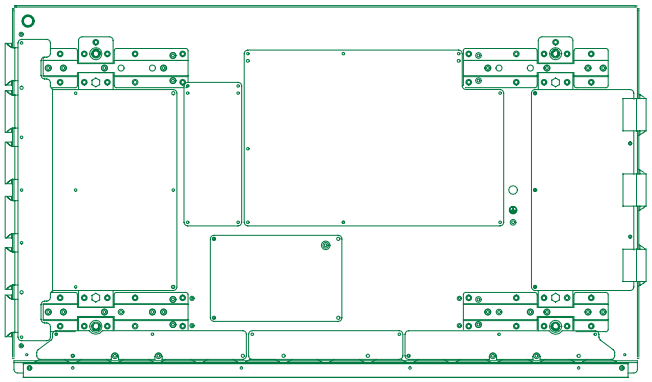


Figure 1-7

50" HDv3

External View
M3 = X Board + Y Board + Logic Board + PSU + SUB PSU

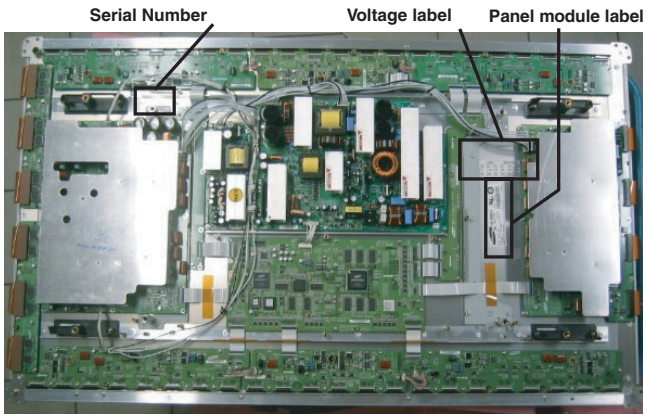


Figure 1-8

Points of Screw Mount

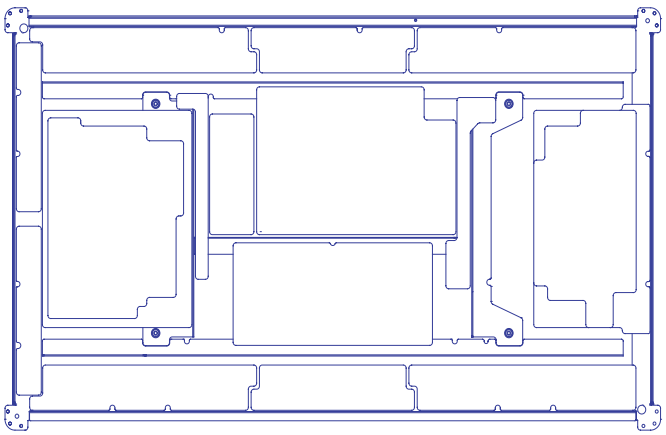


Figure 1-9

1.2 Serial Number

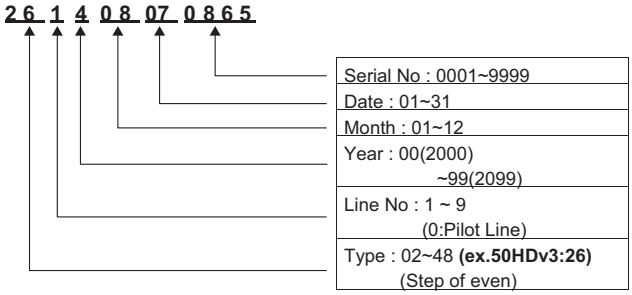

2 6 1 4 0 8 07 0 8 6 5
Serial No : 0001~9999
Date : 01~31
Month : 01~12
Year : 00(2000)
~99(2099)
Line No : 1 ~ 9
(0:Pilot Line)
Type : 02~48 (ex.50HDv3:26)
(Step of even)

Figure 1-10

1.3 Specifications

No	Item	Specification 37" SDV4		Specification 42" SDV2 (ypo6)	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)		852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)		2556 (H) x 480 (V)	
3	Pixel Pitch	0.960 (H) mm x 0.960 (V) mm		1.095 (H) mm x 1.110 (V) mm	
4	Cell Pitch	R	0.320 (H) mm x 0.960 (V) mm	R	0.324 (H) mm x 1.110 (V) mm
		G	0.320 (H) mm x 0.960 (V) mm	G	0.365 (H) mm x 1.110 (V) mm
		B	0.320 (H) mm x 0.960 (V) mm	B	0.406 (H) mm x 1.110 (V) mm
5	Display size	Horizontal 817.92mm x Vertical 460.80mm[32.30 inch x 18.14 inch]		932.940 (H) mm x 532.800(V) mm[36.73 inch x 20.98 inch]	
6	Screen size	Diagonal 37" Color Plasma Display Module		Diagonal 42" Color Plasma Display Module	
7	Screen aspect	16 : 9		16 : 9	
8	Display color	16.77 million colors		16.77 million colors	
9	Viewing angle	Over 160×(Angle with 50% and greater brightness perpendicular to PDP module)		Over 160×(Angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm		982 (W) x 582 (H) x 52.9 (D) mm	
11	Weight	Module 1	About 15.5 kg	Module 1	About 16.6 kg
12	Broadcasting reception-Vertical frequencyand-Video/Logic Interface	PL42SD003C	60Hz/ 50Hz, LVDS	PL42SD003C	60Hz/ 50Hz, LVDS

No	Item	Specification 42" SDV3	
1	Pixel	852 (H) x 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) x 480 (V)	
3	Pixel Pitch	1.095 (H) mm x 1.110 (V) mm	
4	Cell Pitch	R	0.365 (H) mm x 1.110 (V) mm
		G	0.365 (H) mm x 1.110 (V) mm
		B	0.365 (H) mm x 1.110 (V) mm
5	Display size	932.940 (H) mm x 532.800(V) mm[36.73 inch x 20.98 inch]	
6	Screen size	Diagonal 42" Color Plasma Display Module	
7	Screen aspect	16 : 9	
8	Display color	16.77 million colors	
9	Viewing angle	Over 160×(Angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm	
11	Weight	Module 1	About 16.6 kg
12	Broadcasting reception-Vertical frequencyand-Video/Logic Interface	PL42SD003C	60Hz/ 50Hz, LVDS

No	Item	Specification 42" HDV3		Specification 50" HDV3	
1	Pixel	Horizontal 1.024 xVertical 768 pixels(1 pixel = 1 R,G,B cells)		Horizontal 1366 x Vertical 768 pixels(1 pixel = 1 R,G,B cells)	
2	Number of Cells	3072 (H) x 768 (V)		Horizontal 4,098 x Vertical 768 cells	
3	Pixel Pitch	Horizontal 912mm x Vertical 693mm		Horizontal 810mm x mmVertical 810mm	
4	Cell Pitch	R	Horizontal 0.304mm x Vertical 693mm	R	Horizontal 270mm x Vertical 810mm
		G	Horizontal 0.304mm x Vertical 693mm	G	Horizontal 270mm x Vertical 810mm
		B	Horizontal 0.304mm x Vertical 693mm	B	Horizontal 270mm x Vertical 810mm
5	Display size	932.940 (H) mm x 532.800(V) mm[36.73 inch x 20.98 inch]		Horizontal 1106.46mm x Vertical 622.08mm	
6	Screen size	Diagonal 42" Color Plasma Display Module		Diagonal 50" Color Plasma Display Module	
7	Screen aspect	16 : 9		16 : 9	
8	Display color	16.77 million colors		16.77 million colors	
9	Viewing angle	Over 160×(Angle with 50% and greater brightness perpendicular to PDP module)		Over 160×(Angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) x 582 (H) x 52.9 (D) mm		1184(W) x 700 (H) x 60.1 (D) mm	
11	Weight	Module 1	About 18.0 kg	Module 1	About 18.0 kg
12	Broadcasting reception-Vertical frequencyand-Video/Logic Interface	PL42SD003C	60Hz/ 50Hz, LVDS	PL42SD003C	60Hz/ 50Hz, LVDS

2. Safety Instructions, Warnings and Notes

**** To prevent the risks of unit damage, electrical shock and radiation, take the following safety, service, and ESD precautions.**

2.1 Safety instructions ⚠

It is not allowed to operate the FTV-set without glass plate. One function of this glass plate is to absorb Infrared Radiation. Without this glass plate the level of Infrared Radiation produced by the plasma display could damage your eyes.

1. Safety regulations require that during a repair:
   - the set should be connected to the mains via an isolating transformer (in this particular case a transformer of ≥ 800 VA);
   - safety components, indicated by the symbol ⚠ should be replaced by components identical to the original ones;
2. Safety regulations require that after a repair the set must be returned in its original condition. In particular attention should be paid to the following points.
   - Note: The wire trees should be routed correctly and fixed with the mounted cable clamps.
   - The insulation of the mains lead should be checked for external damage.
   - The electrical DC resistance between the mains plug and the secondary side should be checked (only for sets that have mains isolated power supply). This check can be done as follows:
   - unplug the mains cord and connect a wire between the two pins of the mains plug;
   - set the mains switch to the on position (keep the mains cord unplugged!);
   - measure the resistance value between the pins of the mains plug and the metal shielding of the tuner or the aerial connection on the set. The reading should be between 4.5 MΩ and 12 MΩ;
   - switch off the TV and remove the wire between the two pins of the mains plug.
   - The cabinet should be checked for defects to avoid touching of any inner parts by the customer.

2.2 Warnings

1. ESD
   All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD). Careless handling during repair can reduce life drastically. When repairing, make sure that you are connected with the same potential as the mass of the set by a wristband with resistance. Keep components and tools also at this same potential.
2. Available ESD protection equipment:
   - complete kit ESD3 (combining all 6 prior products - small table mat) 4822 310 10671
   - wristband tester 4822 344 13999
3. Never replace modules or other components while the unit is switched on.
4. When making settings, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

2.3 Handling Precautions for Plasma Display

- PDP module use high voltage that is dangerous to human. Before operating PDP, always check the dust to prevent short circuit. Be careful touching the circuit device when power is on.
- PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- PDP module has a lot of electric devices. Service engineer must wear equipment(for example, earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. Operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is off. Operator must wait for discharging of remaining voltage during at least 1 minute.

2.4 Safety Precautions for Service (Handling, prevention of a electrical shock)

2.4.1 (Safety Precautions)

- Before replacing a board, discharge forcibly
- The remaining electricity from board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operations.
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.
- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuffs including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change : Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, It cause danger on safety. And, If you change the design or insert, Manufactor guarantee will be not effect. .
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between parts and circuit board. Check the cord of AC power preparing damage.
- Product Safety Mark: Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned off, before next repair..
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

2.4.2 (Precaution when repairing ESD)

- There is ESD which is easily damaged by electrostatics.(for example Integrated circuit, FET) Electrostatic damage rate of product will be reduced by the following technics
- Before handling semiconductor parts/assembly, must remove positive electric by ground connection, or must wear the antistatic wrist-belt and ring. (It must be operated after removing dust on it - It comes under precaution of electric shock.)

- After removing ESD assembly, put on it with aluminum stuff on the conductive surface to prevent charging.
- Do not use chemical stuff using Freon. It generates positive electric that can damage ESD.
- Must use a soldering device for ground-tip when soldering or de-soldering ESD.
- Must use anti-static solder removal device. Most removal device do not have antistatic which can charge a enough positive electric enough damaging ESD.
- Before removeing the protective material from the lead of a new ESD, bring the protective material into contact with the chassis or assembly that the ESD is to be installed on.
- When handing an unpacked ESD for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the ESD.
- Do not take a new ESD from the protective case until the ESD is ready to be installed. Most ESD have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminum)

2.5 Notes

A glass plate is positioned before the plasma display. This glass plate can be cleaned with a slightly humid cloth. If due to circumstances there is some dirt between the glass plate and the plasma display panel it is recommended to do some maintenance by a qualified service employee only.

2.5.1 Notes on safe handling of the plasma display

Notes to follow during service

- The work procedures shown with the Note indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.
- Before starting the work, secure a sufficient working space.
- At all times other than when adjusting and checking the product, be sure to turn OFF the main POWER switch and disconnect the power cable from the power source of the display (jig or the display itself) during servicing.
- To prevent electric shock and breakage of pwb, start the servicing work at least 30 seconds after the main power bas been turned off. Especially when installing and removing the power supply pwb and the SUS pwb in which high voltages are applied, start servicing at least 2 minutes after the main power bas been turned off.
- While the main power is on, do not touch any parts or circuits other than the ones specified. The high voltage power supply block within the PDP module has a floating ground. If any connection other than the one specified is made between the measuring equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.
- When installing the PDP module in, and removing it from the packing carton, be sure to have at least two persons
- perform the work white being careful to ensure that the flexible printed-circuit cable of the PDP module does not
- get caught by the packing carton.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in, the surface of the panel being scratched by foreign matter.
- When handling the circuit pwb, be sure to remove static electricity from your body before handling the circuit pwb.
- Be sure to handle the circuit pwb by holding the large parts as the heat sink or transformer. Failure to observe this precaution may result in the occurrence of an abnormality in the soldered areas.
- Do not stack the circuit pwb. Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed. All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.
- Perform a safety check when servicing is completed. Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original

3. Directions For Use

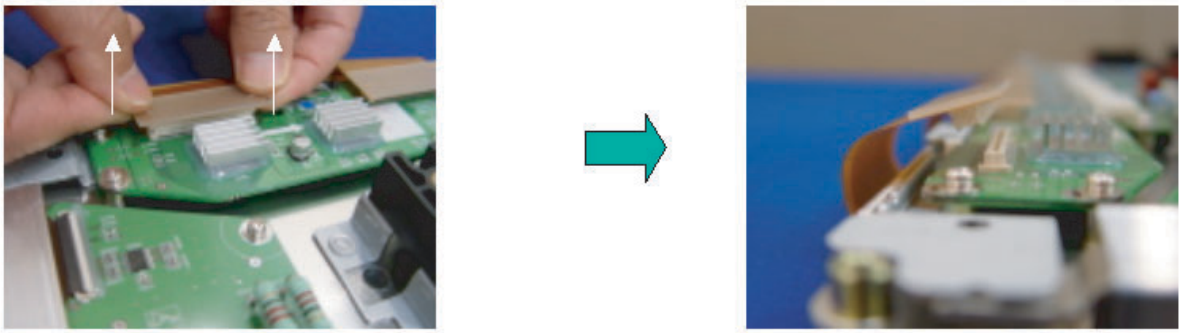
Not applicable

4. Mechanical Instruction

4.1 Disassembling / Re-asssembling

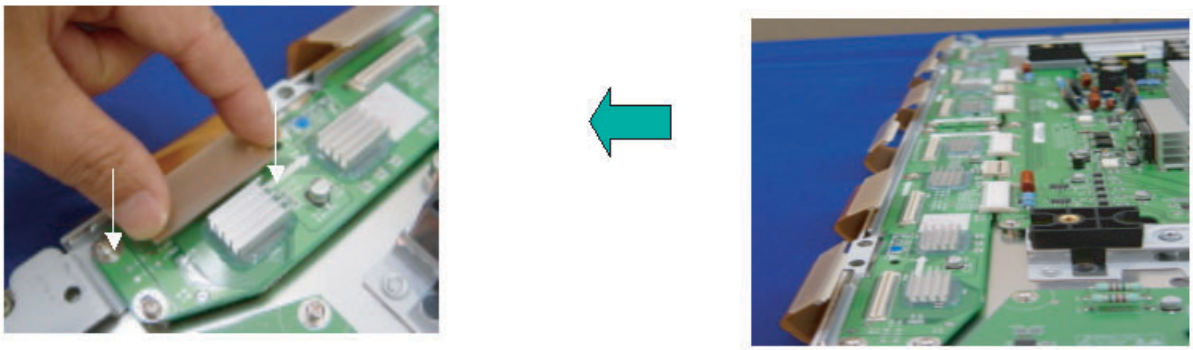
4.1.1 Disassembling & Re-assembling of FPC (Flexible Printed Circuit) and Y-Buffer (Upper and Lower)

1. Removal procedure



- Pull out the FPC from Connector by holding the lead of the FPC with both hands.

2. Assembling procedures

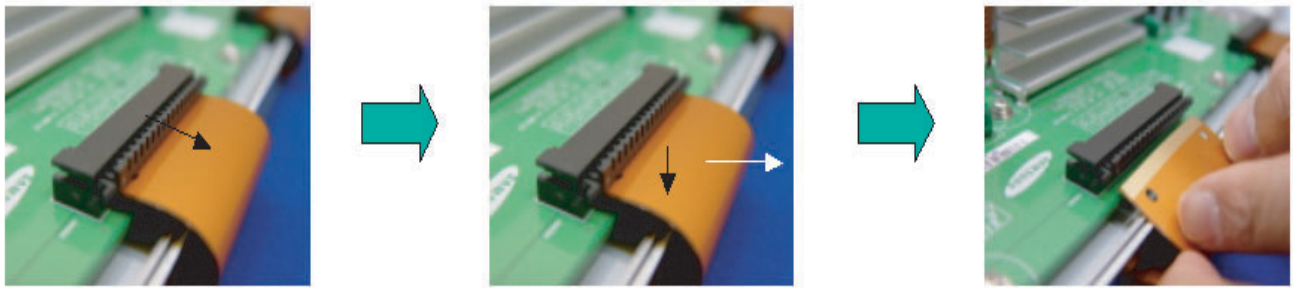


- Push the lead of FPC with same force on both sides into the connector.

Notice: Be careful do not get a damage on the connector pin during connecting by mistake.

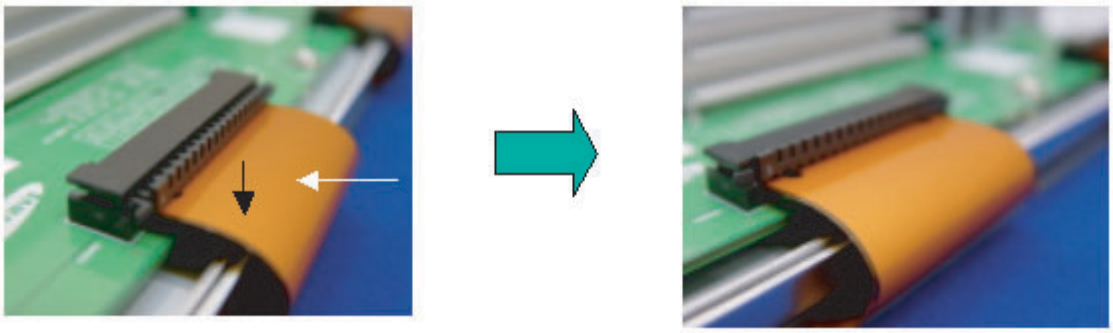
4.1.2 Assembling & Disassembling of Flat Cable Connector of X-main Board

1. **Disassembling Procedure**



- Pull out the clamp of connector.
- Pull Flat cable out press down lightly.
- Turn the Flat cable reversely.

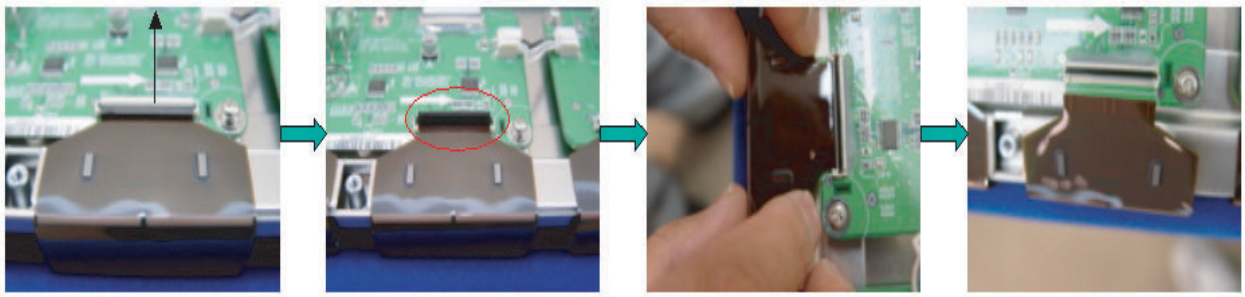
2. **Assembling Procedures**



- Put the Flat cable into the connector press down lightly until locking sound (“Click.“) comes out.

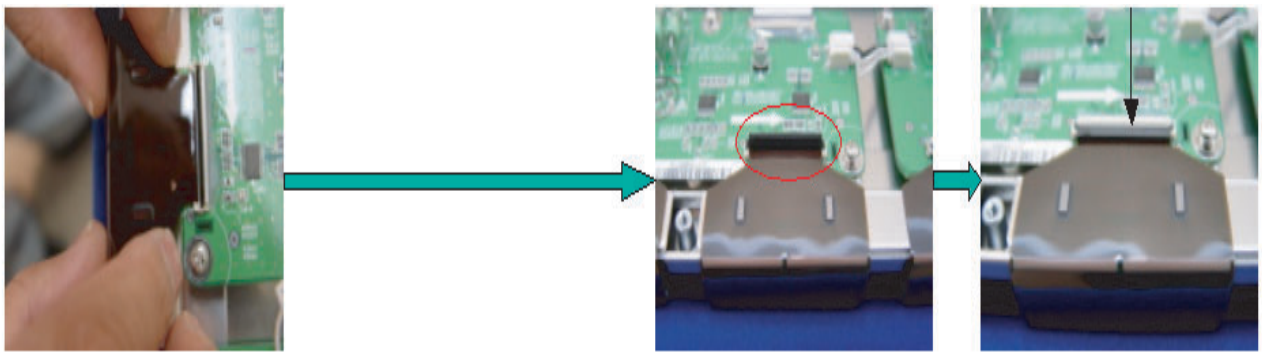
4.1.3 Assembling & Disassembling the FFC and TCP form Connector

1. **Disassembling of TCP**



- Open the clamp carefully.
- Pull the TCP out from connector.

2. **Assembling of TCP**

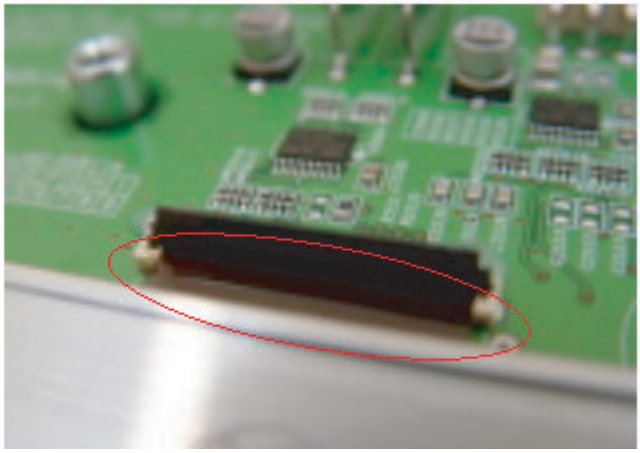


- Put the TCP into the Connector carefully
- Close the clamp completely.
  (The sound “Click.” comes out.)

Notice:

- 1) Checking whether the foreign material is on the Connector inside before assembling of TCP.
- 2) Be careful do not get a damage on the board by ESD during handling of TCP.

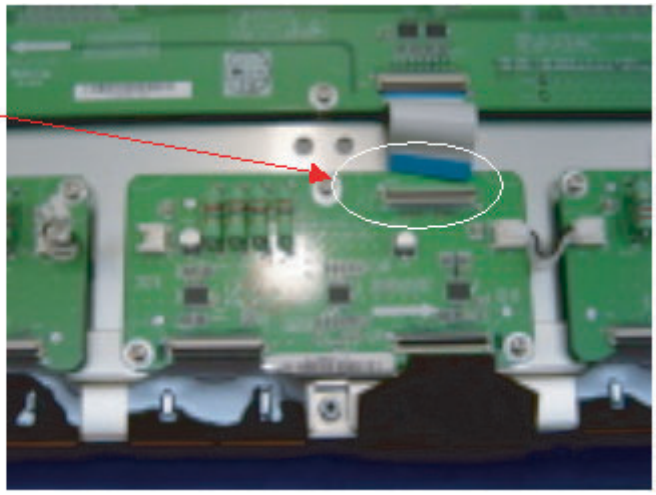
3. **Misassembling of TCP**



- The misassembling of TCP is the cause of defect.

4. **Assembling & Disassembling of FFC**

The procedure of assembling and disassembling of FFC is same as TCP



- This is the photo of the assembling of FFC.

4.1.4Exchange of LBE, LBF, LBG board

Photo 1

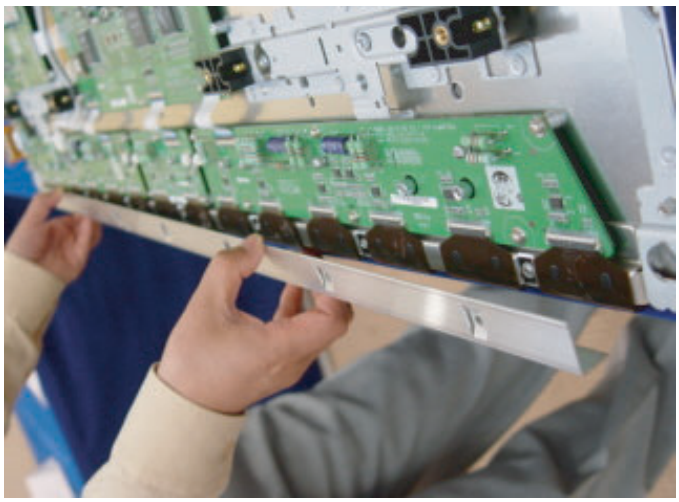


Photo 2 - 42" SDv2

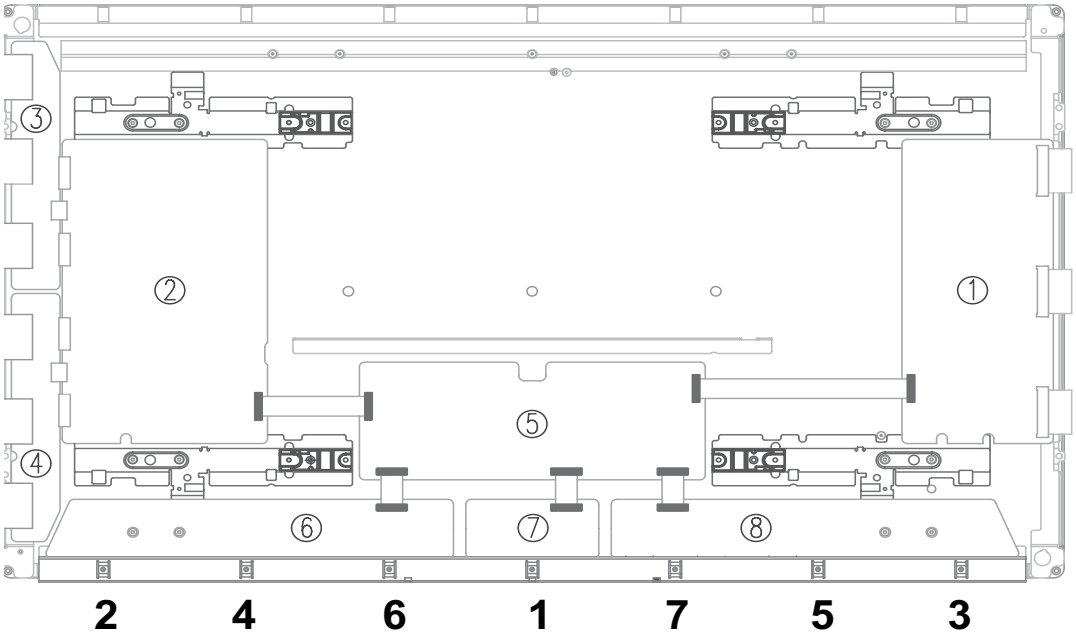


Photo 2 - 42" SDv3

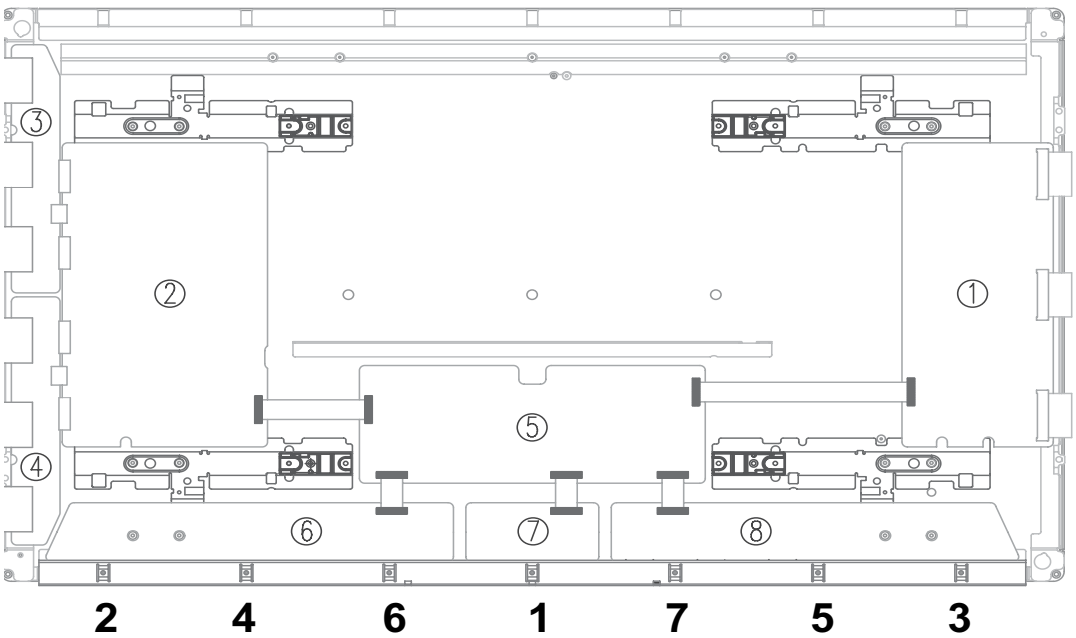


Photo 2 - 42" HDv3

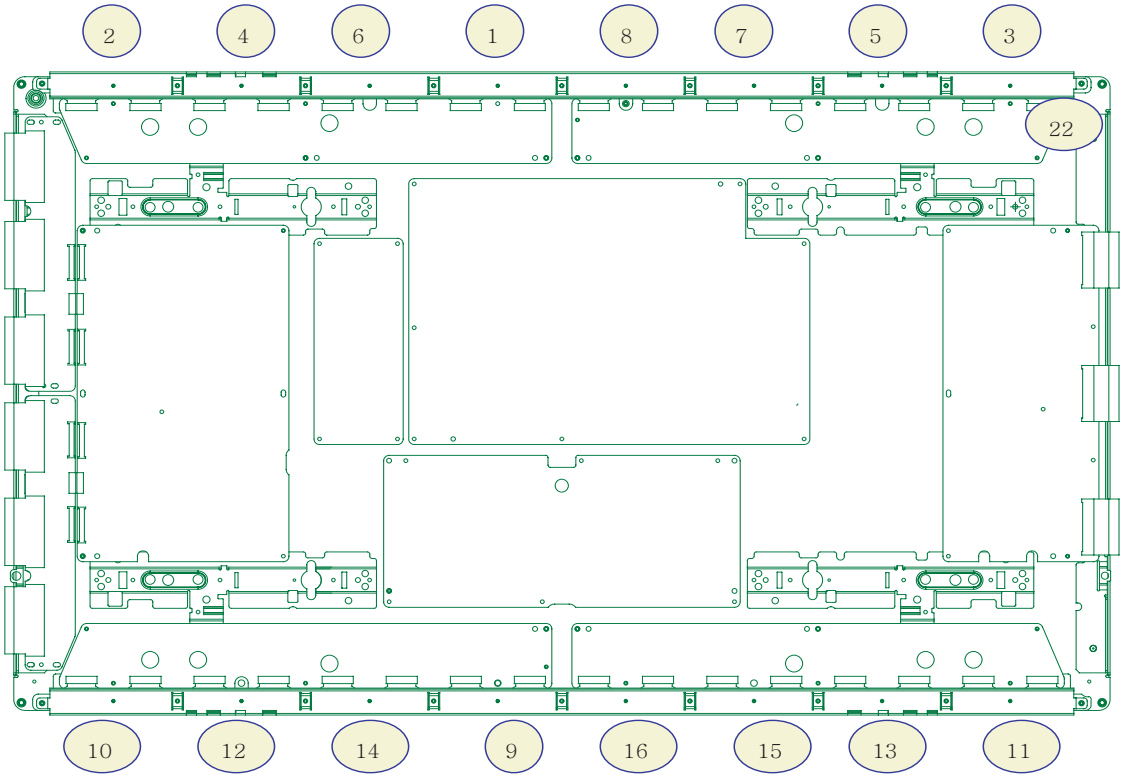


Photo 2 - S37" SDv4

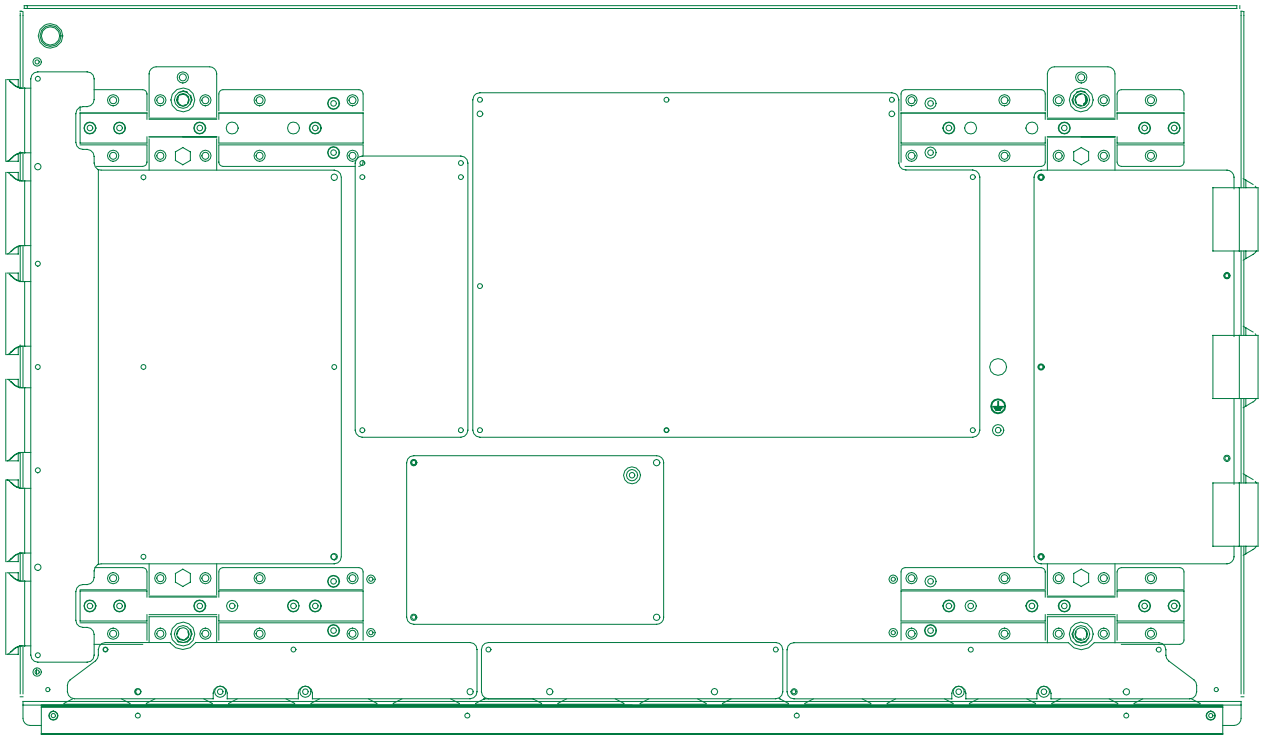
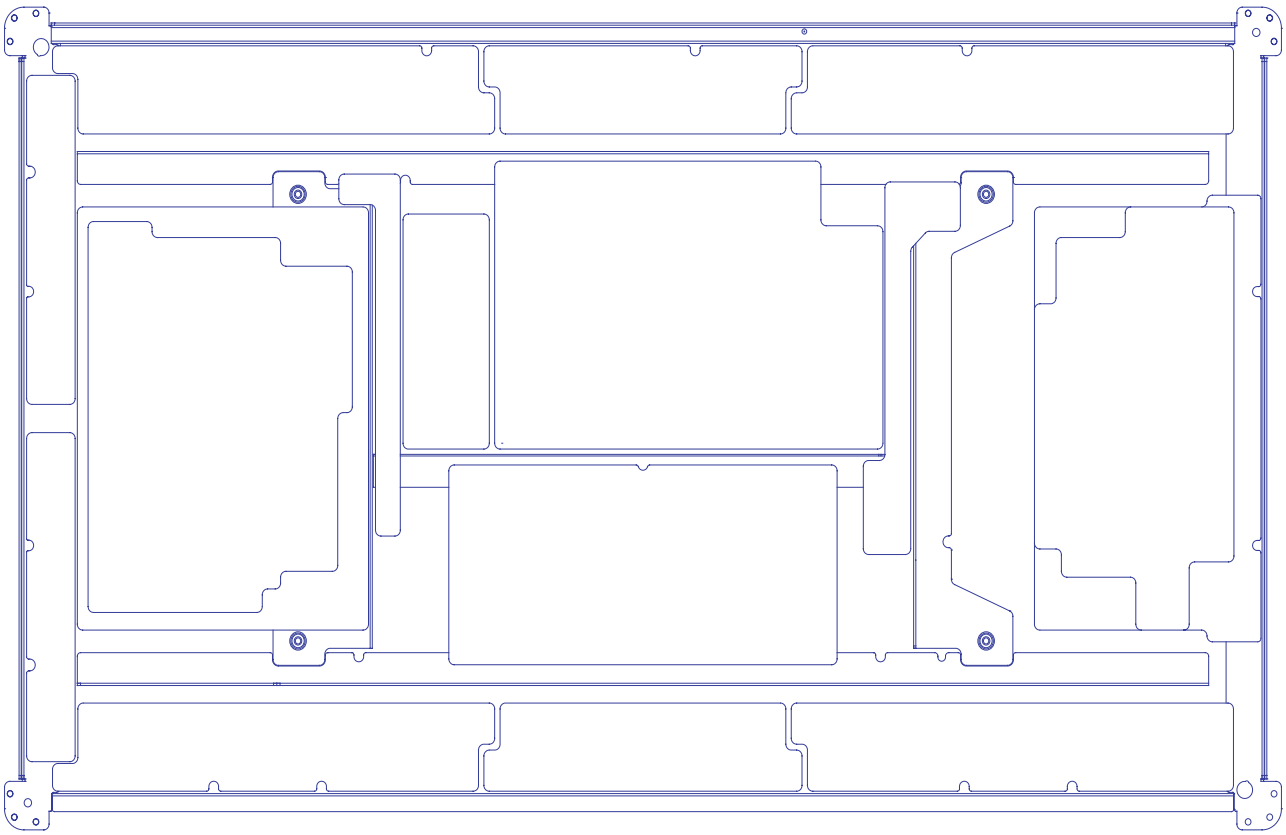


Photo 2 - 50" HDv3

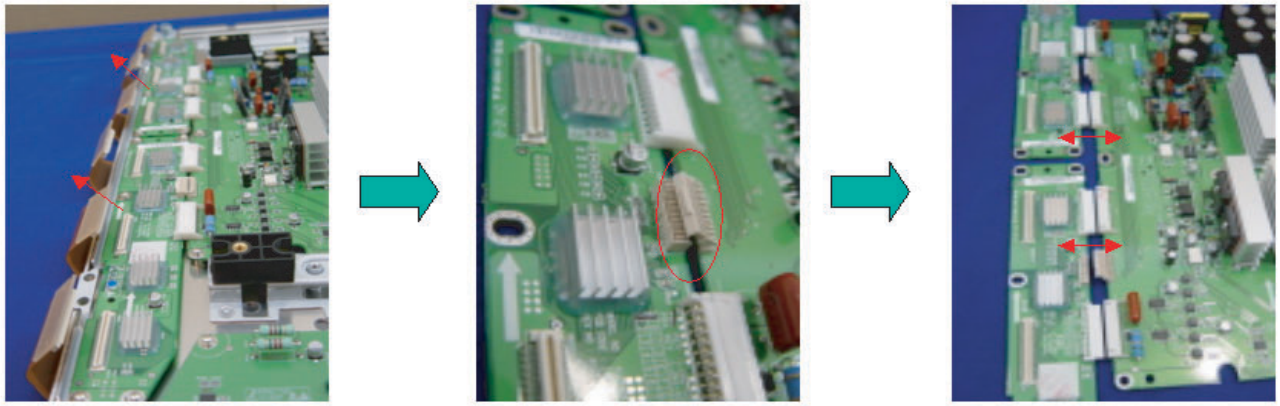


1. 42" SDv3 - Remove the screws in order of 2-3-5-7-1-4-6 and 10-11-13-16-9-12-14 for HD from heat sink and then get rid of heat sink. (Photo 1)
   42" HDv3, S37" SDv4, 50" HDv3
   - Remove the screws in order of Center - Left Side - Right Side from heat sink and then get rid of heat sink. (Photo 1)
2. Remove the TPC, FFC and power cable from the connectors.
3. Remove all the screws from defected board.
4. Remove the defected board.
5. Replace the new board and then screw tightly.
6. Get rid of the foreign material from the connector.
7. Connect the TCP, FFC and power cable to the connector.
8. Reassemble the TCP heat sink.
9. 42" SDv3 - Screw in order of 4-1-7-6-5-3-2 and 12-9-15-14-13-11-10 for HD. (Photo 2) 42" HDv3, S37" SDv4, 50" HDv3
   - Screw in order of Right Side - Left Side - Center (Photo 2)

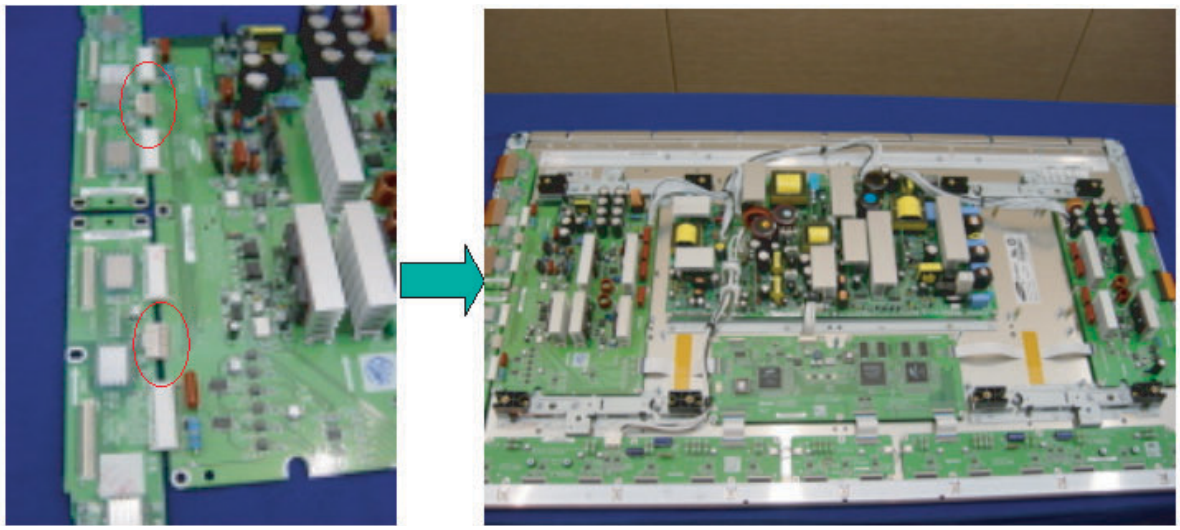
   If you screw too tightly, it is possible to get damage on the Driver IC of TCP.

4.1.5 Exchange YBU, YBL and YM board

1. Separate all the FPC connector of YBU (Y-Buffer upper) and YBL (Lower). (Photo 1)
2. Separate all the connector of CN5001 and CN5008 from Y-Main.
3. Loosen all the screws of YBU, YBL and YM.
4. Remove the board from chassis.
5. Remove the connector of CN5006 and CN5007 among YBU, YBL and YM.
6. Remove the YBL and YBU from Y-main.
7. Replace the defected board.



8. Reassemble the YBU and YBL to the Y-Main.
9. Connect the connector of CN5006 and CN5007 among YBU, YBL and YM.
10. Arrange the board on the chassis and then screw to fix.
11. Connect the FPC and YM of panel to the connector.
12. Supply the electric power to the module and then check the waveform of board.
13. Turn off the power after the waveform is adjusted.



5. Diagnostic software

5.1 Repair tools

1.) 3122 785 90581 = Foam buffers
2.) Compair connector: 3122 785 90800
3.) V2 jig 3122 785 90760
4.) V3 jig 3122 785 90770

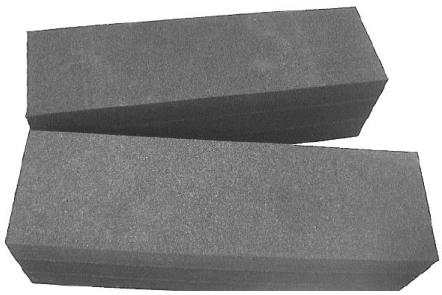


Figure 5-1 Foam buffers for PDP

Figure 5-2 3122 785 90760

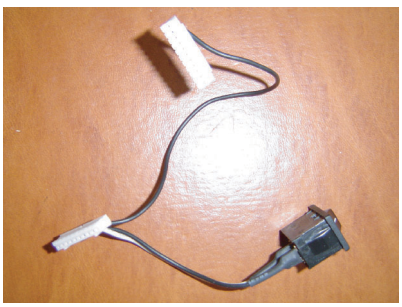


Figure 5-3 3122 785 90770

5.2 Repair Scenario

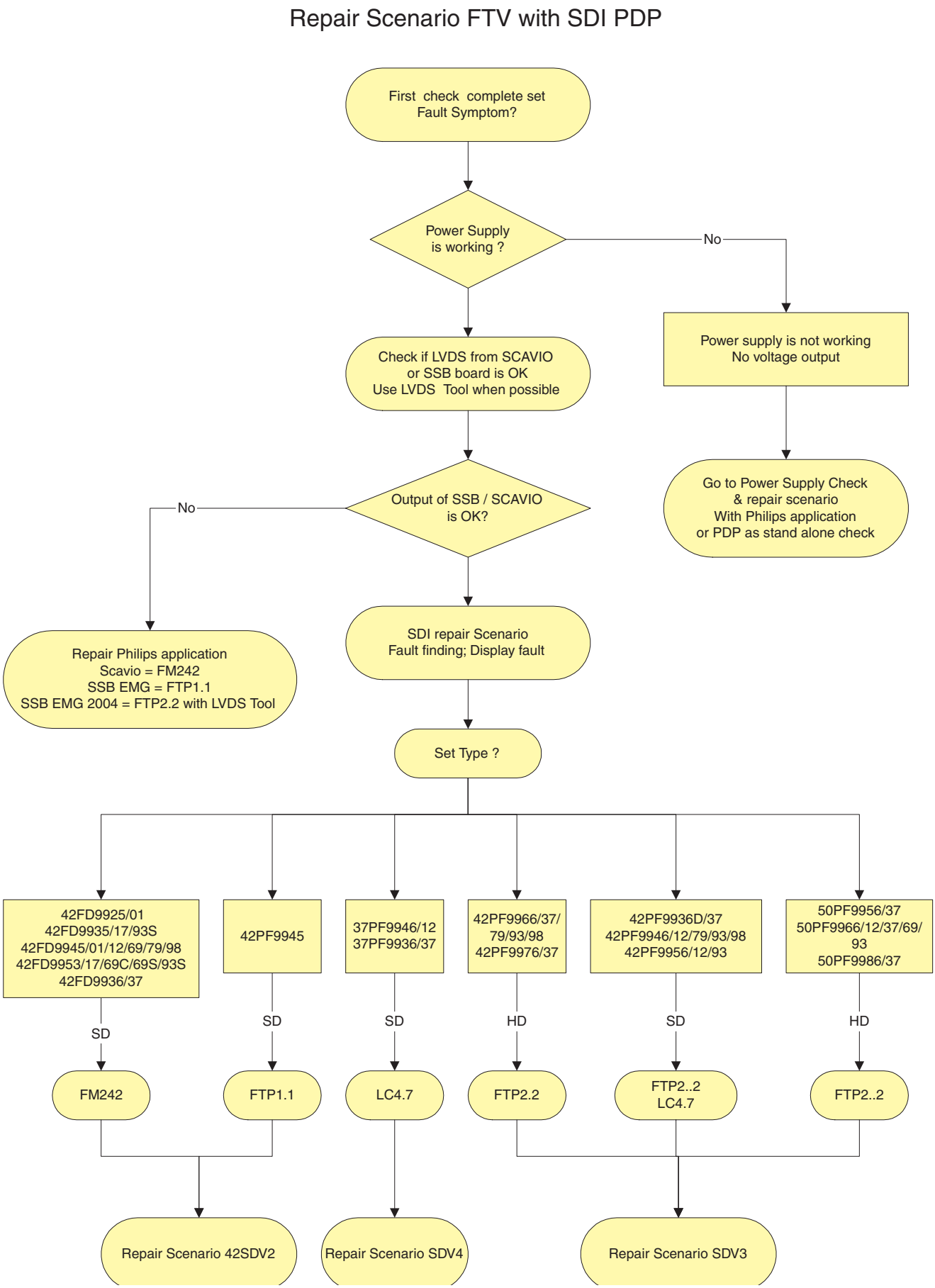


Figure 5-4

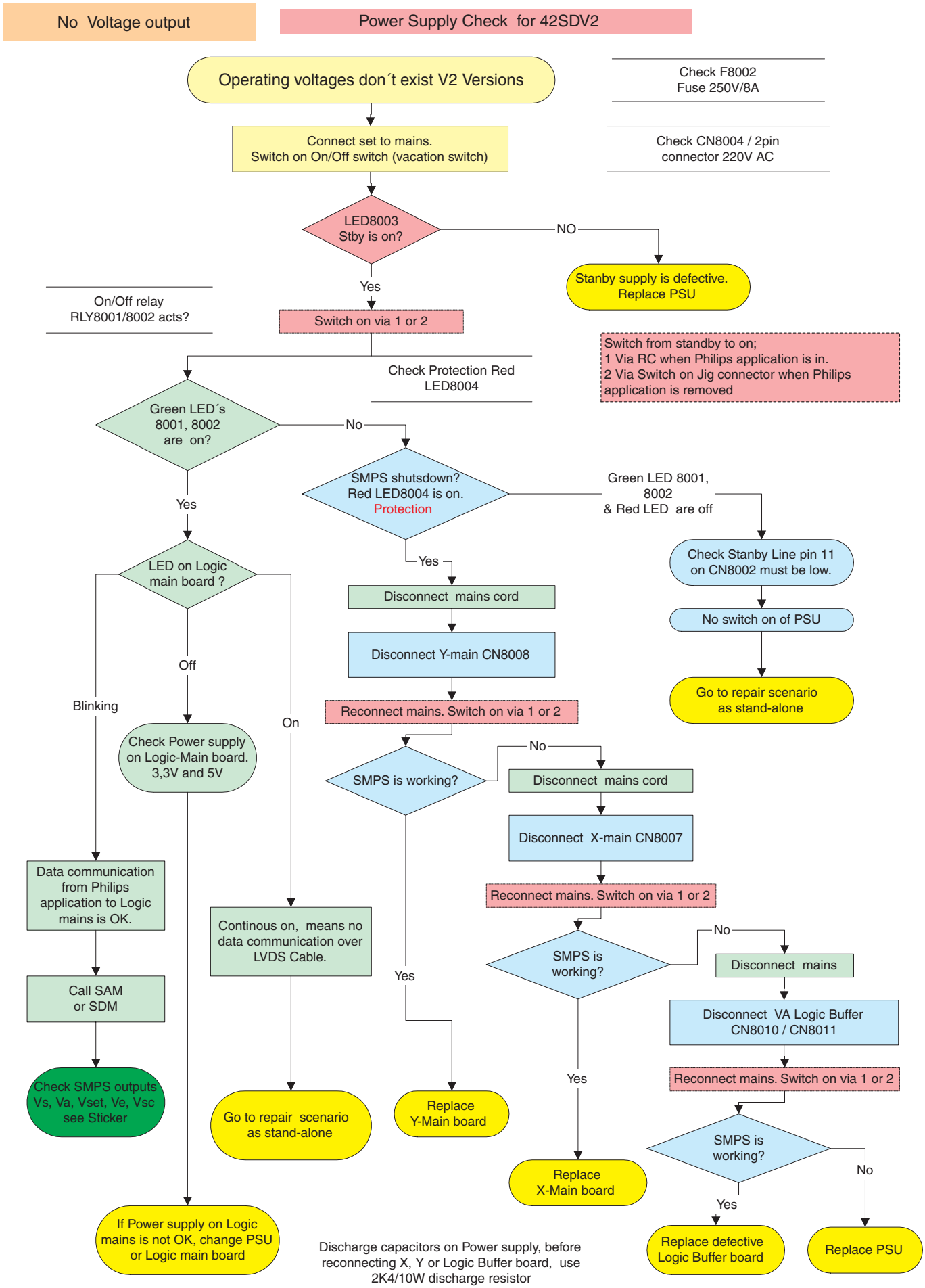

No Voltage output
Power Supply Check for 42SDV2
Operating voltages don´t exist V2 Versions
Check F8002
Fuse 250V/8A
Connect set to mains.
Switch on On/Off switch (vacation switch)
Check CN8004 / 2pin
connector 220V AC
LED8003
Stby is on?
NO
Yes
Stanby supply is defective.
Replace PSU
On/Off relay
RLY8001/8002 acts?
Switch on via 1 or 2
Switch from standby to on;
1 Via RC when Philips application is in.
2 Via Switch on Jig connector when Philips
application is removed
Check Protection Red
LED8004
Green LED´s
8001, 8002
are on?
No
Yes
SMPS shutsdown?
Red LED8004 is on.
Protection
Green LED 8001,
8002
& Red LED are off
LED on Logic
main board ?
Yes
Disconnect mains cord
Disconnect Y-main CN8008
Reconnect mains. Switch on via 1 or 2
Check Stanby Line pin 11
on CN8002 must be low.
No switch on of PSU
Go to repair scenario
as stand-alone
Blinking
Off
On
Check Power supply
on Logic-Main board.
3,3V and 5V
SMPS is working?
No
Disconnect mains cord
Disconnect X-main CN8007
Reconnect mains. Switch on via 1 or 2
Data communication
from Philips
application to Logic
mains is OK.
Continous on, means no
data communication over
LVDS Cable.
SMPS is
working?
No
Disconnect mains
Disconnect VA Logic Buffer
CN8010 / CN8011
Reconnect mains. Switch on via 1 or 2
Call SAM
or SDM
Yes
Yes
Yes
Check SMPS outputs
Vs, Va, Vset, Ve, Vsc
see Sticker
Go to repair scenario
as stand-alone
Replace
Y-Main board
Replace
X-Main board
SMPS is
working?
No
Yes
If Power supply on Logic
mains is not OK, change PSU
or Logic main board
Discharge capacitors on Power supply, before
reconnecting X, Y or Logic Buffer board, use
2K4/10W discharge resistor
Replace defective
Logic Buffer board
Replace PSU

Figure 5-5

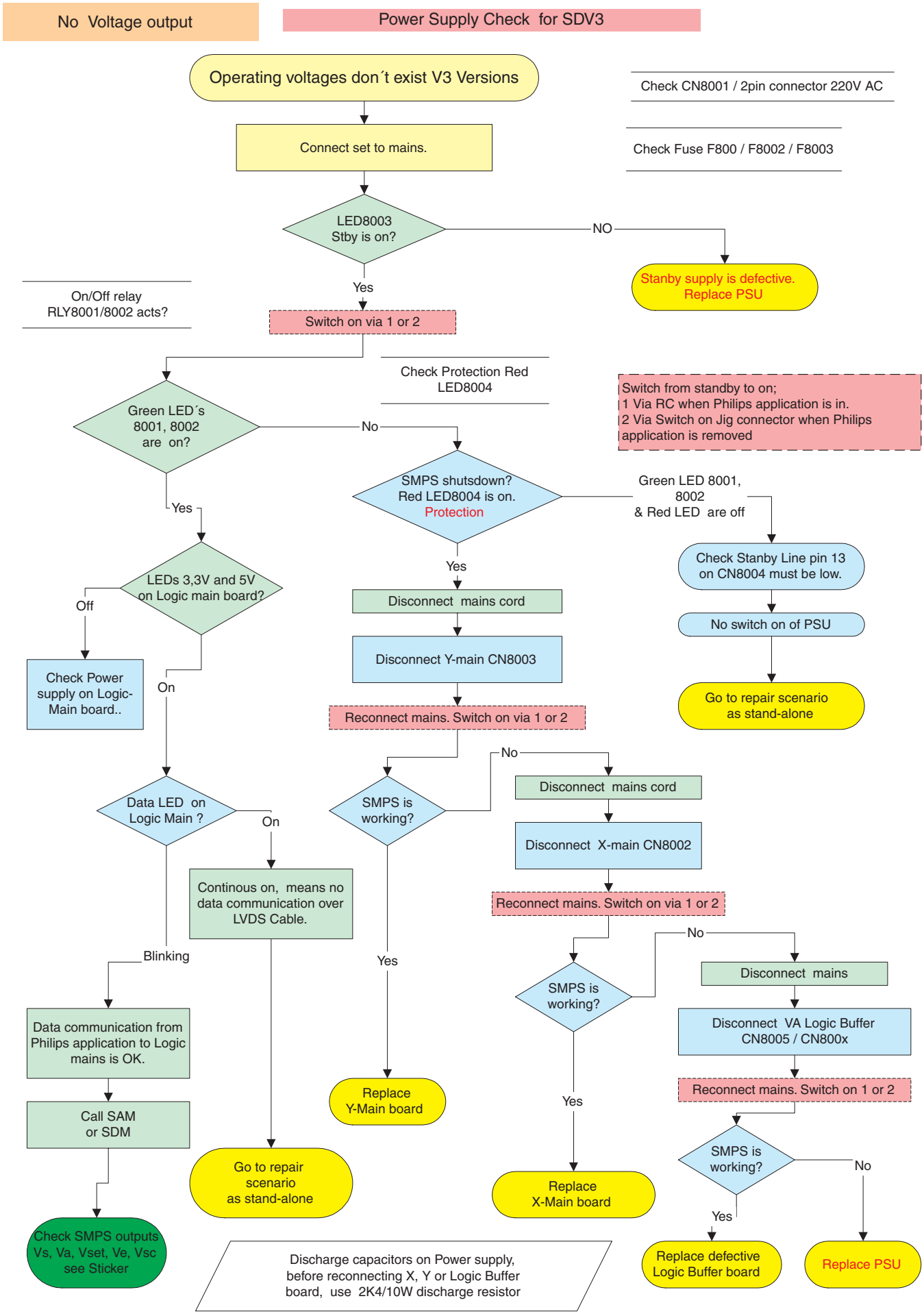

No Voltage output
Power Supply Check for SDV3
Operating voltages don´t exist V3 Versions
Connect set to mains.
LED8003 Stby is on?
NO
Stanby supply is defective. Replace PSU
Yes
On/Off relay RLY8001/8002 acts?
Switch on via 1 or 2
Check CN8001 / 2pin connector 220V AC
Check Fuse F800 / F8002 / F8003
Check Protection Red LED8004
Switch from standby to on;
1 Via RC when Philips application is in.
2 Via Switch on Jig connector when Philips application is removed
Green LED´s 8001, 8002 are on?
No
Yes
SMPS shutsdown? Red LED8004 is on. Protection
Green LED 8001, 8002 & Red LED are off
Check Stanby Line pin 13 on CN8004 must be low.
No switch on of PSU
Go to repair scenario as stand-alone
LEDs 3,3V and 5V on Logic main board?
Off
On
Check Power supply on Logic-Main board..
Yes
Disconnect mains cord
Disconnect Y-main CN8003
Reconnect mains. Switch on via 1 or 2
Data LED on Logic Main ?
On
Blinking
SMPS is working?
No
Yes
Disconnect mains cord
Disconnect X-main CN8002
Reconnect mains. Switch on via 1 or 2
Continous on, means no data communication over LVDS Cable.
Data communication from Philips application to Logic mains is OK.
Call SAM or SDM
Check SMPS outputs Vs, Va, Vset, Ve, Vsc see Sticker
Replace Y-Main board
Go to repair scenario as stand-alone
SMPS is working?
No
Yes
Disconnect mains
Disconnect VA Logic Buffer CN8005 / CN800x
Reconnect mains. Switch on 1 or 2
Replace X-Main board
SMPS is working?
No
Yes
Replace defective Logic Buffer board
Replace PSU
Discharge capacitors on Power supply, before reconnecting X, Y or Logic Buffer board, use 2K4/10W discharge resistor

Figure 5-6

Repair Scenario SDI PDP panels as stand alone V2 versions

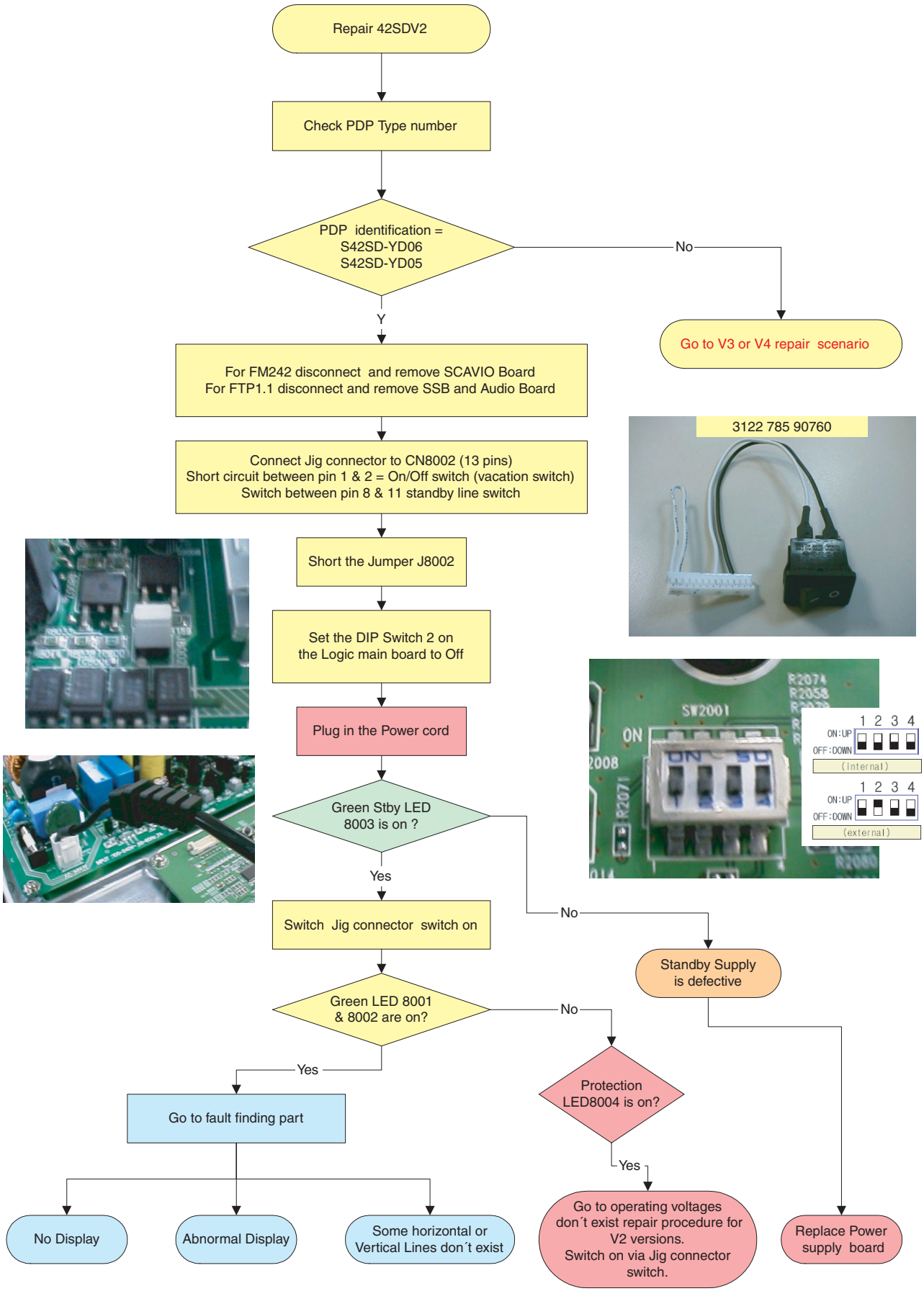

Repair 42SDV2
Check PDP Type number
PDP identification = S42SD-YD06 S42SD-YD05
No
Y
Go to V3 or V4 repair scenario
For FM242 disconnect and remove SCAVIO Board
For FTP1.1 disconnect and remove SSB and Audio Board
Connect Jig connector to CN8002 (13 pins)
Short circuit between pin 1 & 2 = On/Off switch (vacation switch)
Switch between pin 8 & 11 standby line switch
3122 785 90760
Short the Jumper J8002
Set the DIP Switch 2 on the Logic main board to Off
Plug in the Power cord
SW2001
ON
1 2 3 4
ON:UP
OFF:DOWN
(internal)
(external)
Green Stby LED 8003 is on ?
Yes
No
Switch Jig connector switch on
Standby Supply is defective
Green LED 8001 & 8002 are on?
No
Yes
Protection LED8004 is on?
Yes
Go to fault finding part
No Display
Abnormal Display
Some horizontal or Vertical Lines don´t exist
Go to operating voltages don´t exist repair procedure for V2 versions. Switch on via Jig connector switch.
Replace Power supply board

Figure 5-7

Repair Scenario SDI PDP panels as stand alone V3 & V4 versions

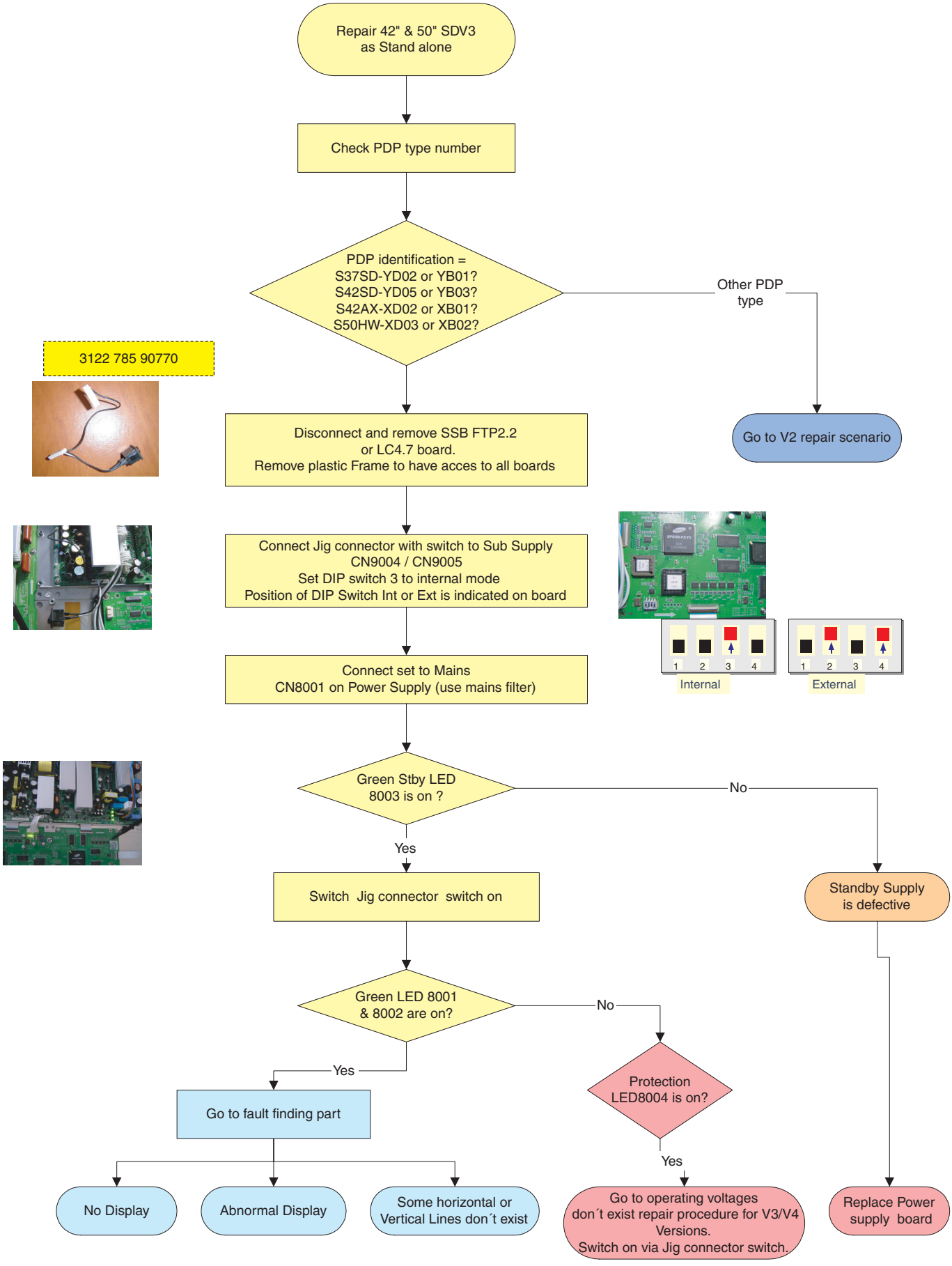


Figure 5-8

Fault Symptoms

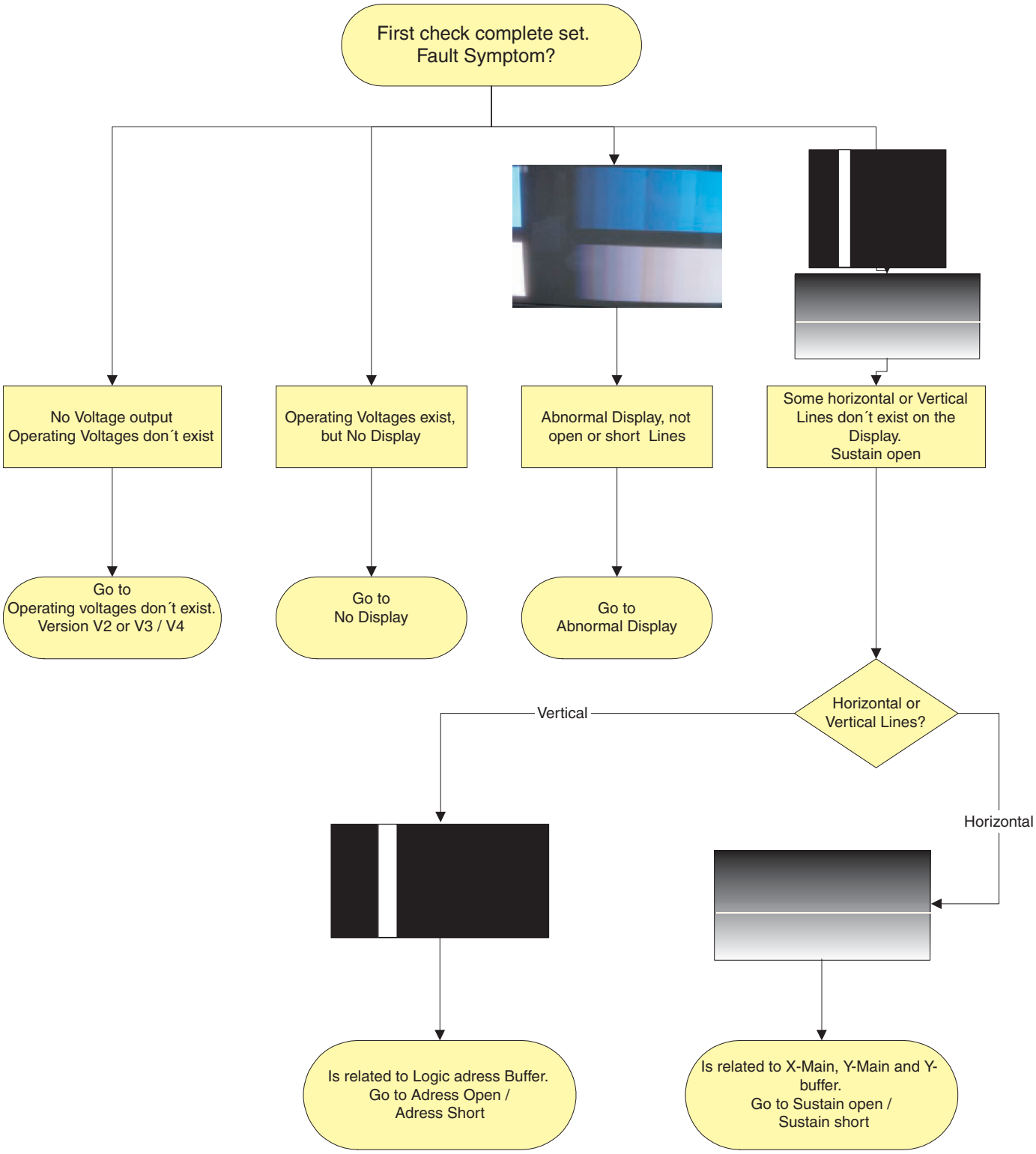


Figure 5-9

No Display

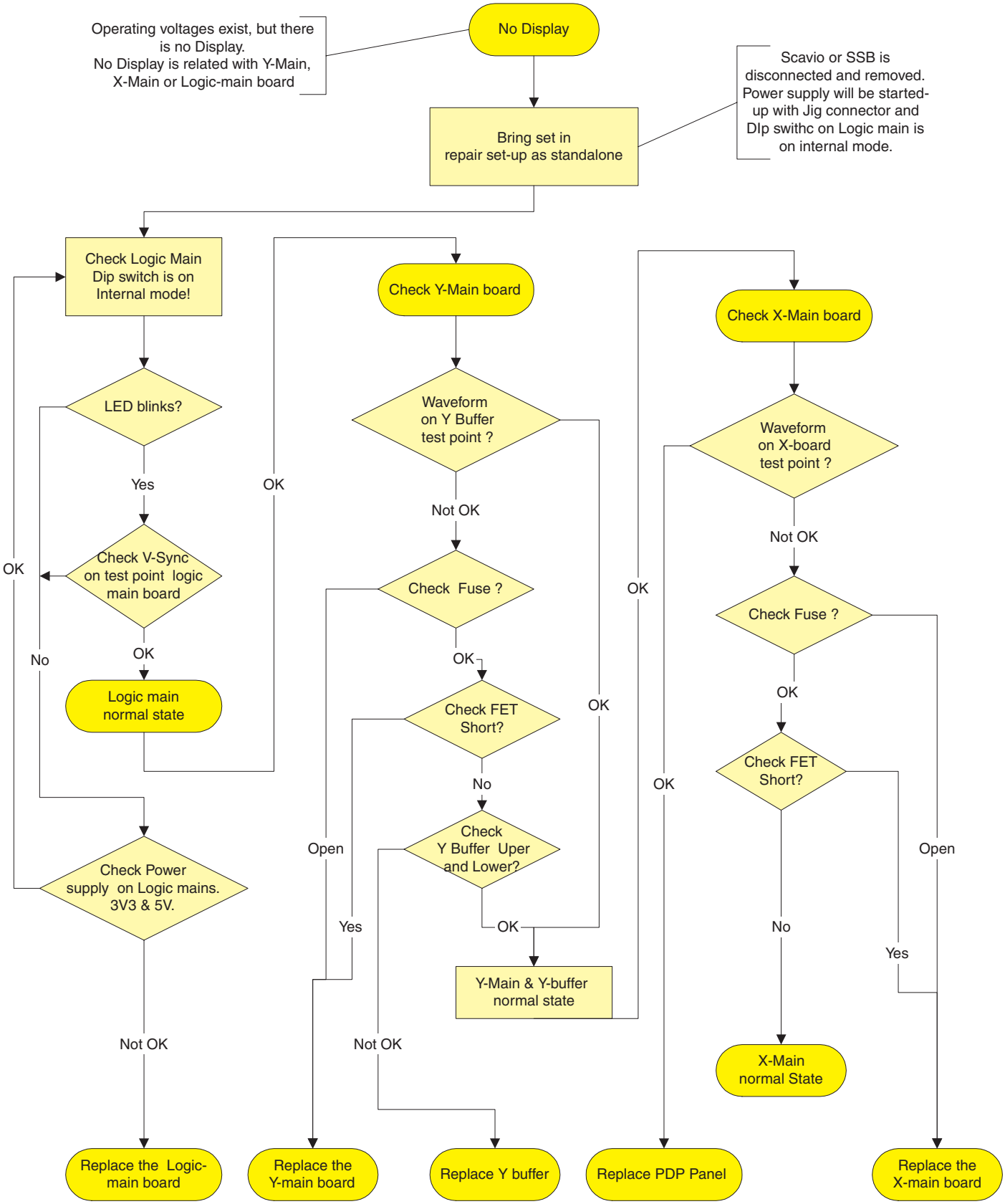


Figure 5-10

Abnormal Display

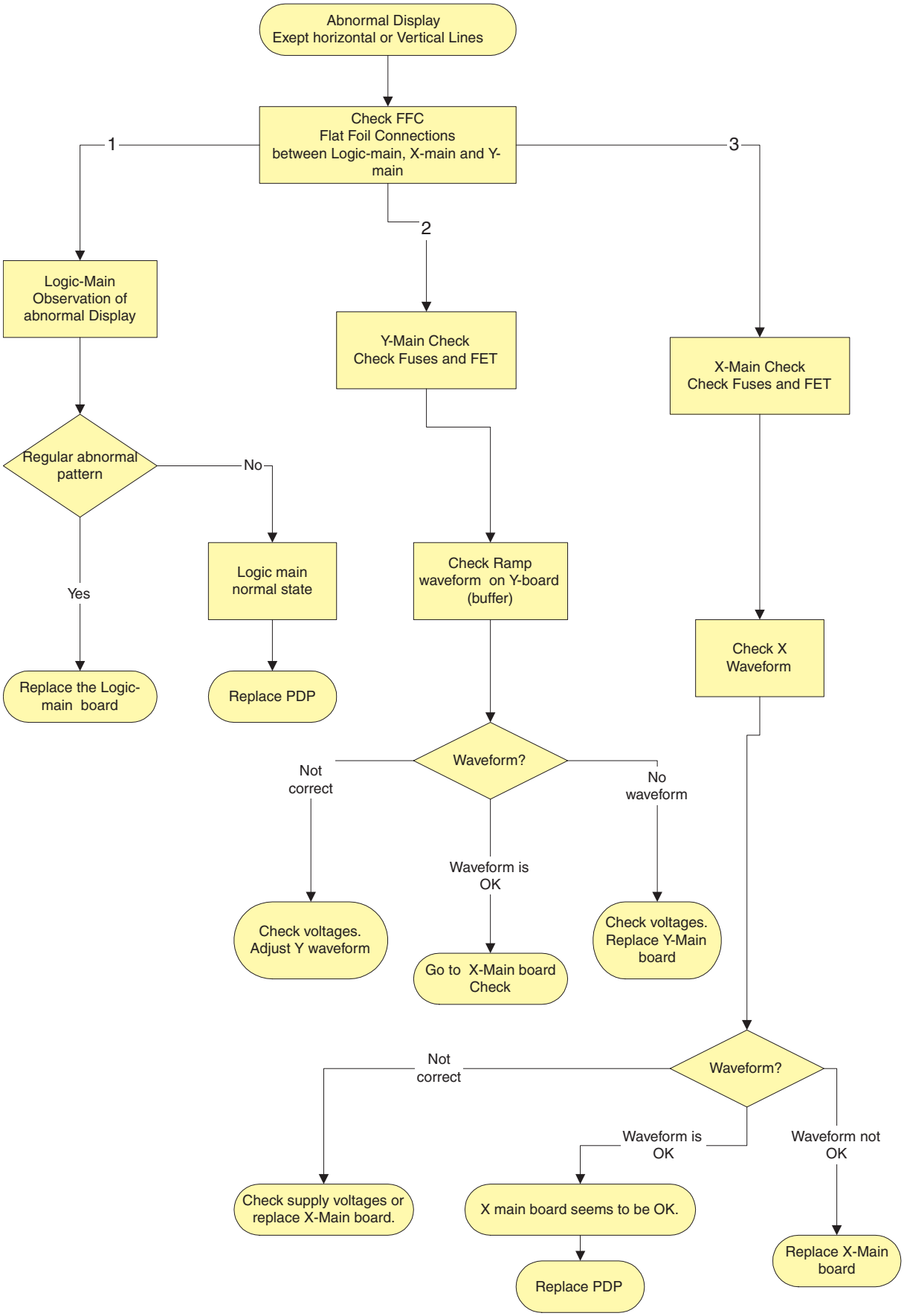


Figure 5-11

Some horizontal lines don´t exist on the Display. Sustain open or short

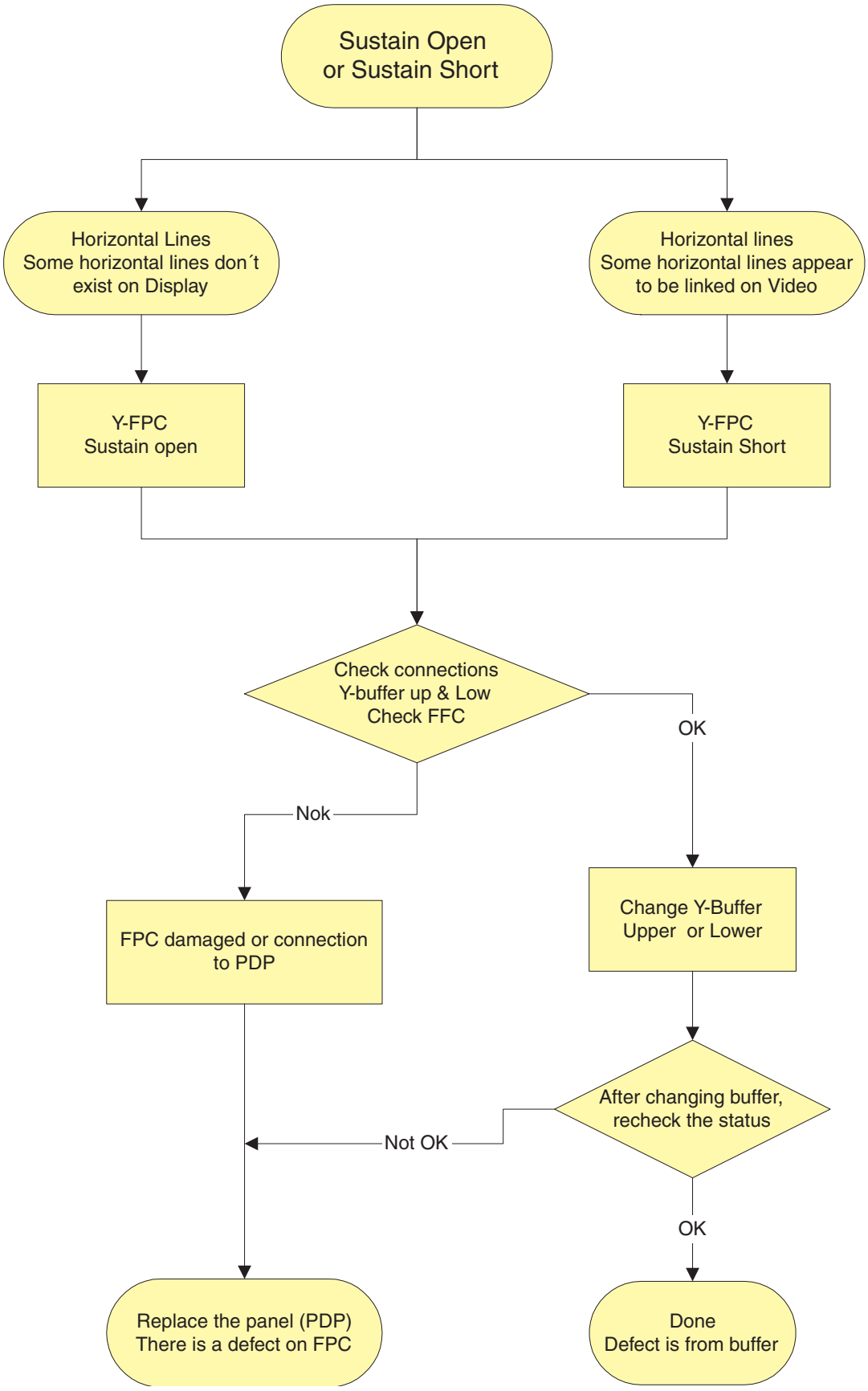


Figure 5-12

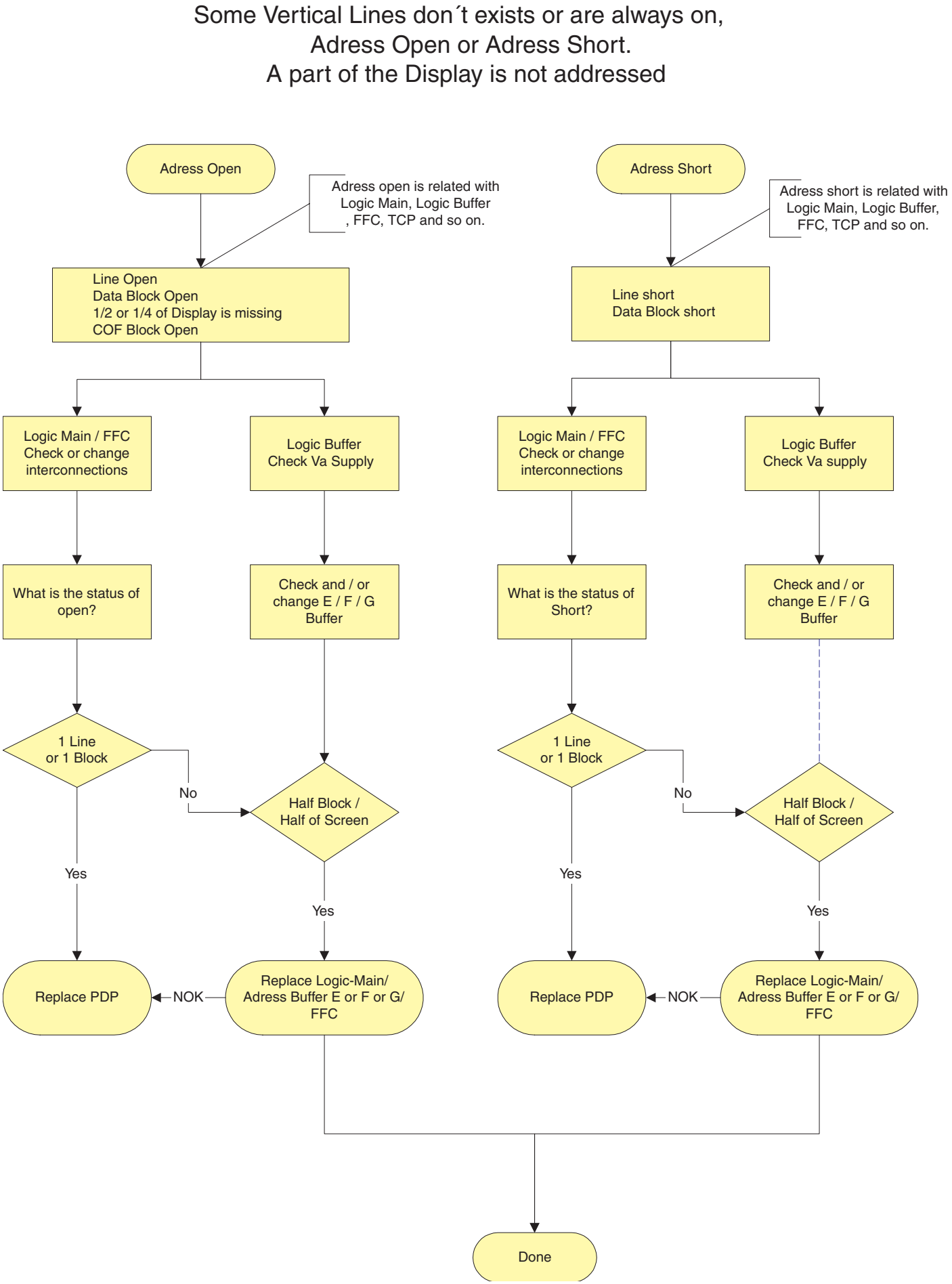
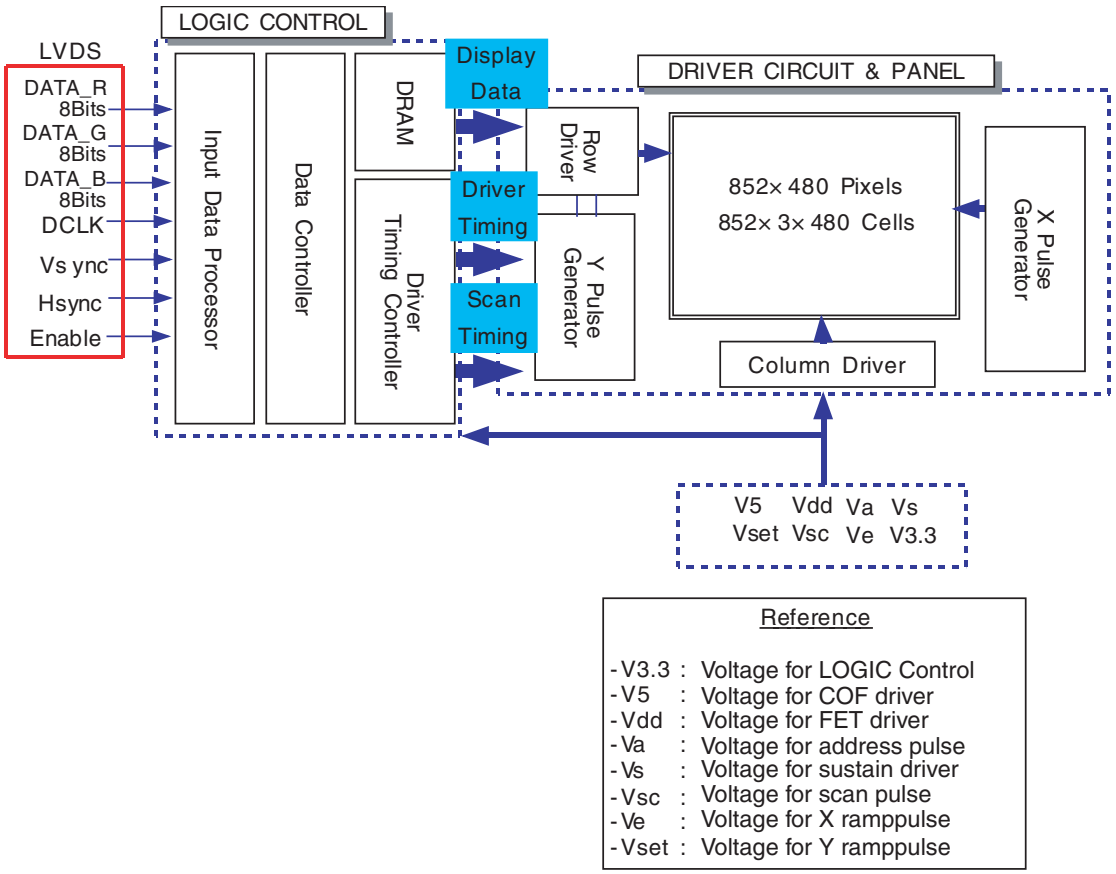

Some Vertical Lines don´t exists or are always on,
Adress Open or Adress Short.
A part of the Display is not addressed
Adress Open
Adress open is related with Logic Main, Logic Buffer , FFC, TCP and so on.
Line Open
Data Block Open
1/2 or 1/4 of Display is missing
COF Block Open
Logic Main / FFC Check or change interconnections
Logic Buffer Check Va Supply
What is the status of open?
Check and / or change E / F / G Buffer
1 Line or 1 Block
No
Half Block / Half of Screen
Yes
Yes
Replace PDP
NOK
Replace Logic-Main/ Adress Buffer E or F or G/ FFC
Adress Short
Adress short is related with Logic Main, Logic Buffer, FFC, TCP and so on.
Line short
Data Block short
Logic Main / FFC Check or change interconnections
Logic Buffer Check Va supply
What is the status of Short?
Check and / or change E / F / G Buffer
1 Line or 1 Block
No
Half Block / Half of Screen
Yes
Yes
Replace PDP
NOK
Replace Logic-Main/ Adress Buffer E or F or G/ FFC
Done

Figure 5-13

6. Block Diagrams, Testpoint Overview, and Waveforms

6.1 Block Diagram for Logic circuit

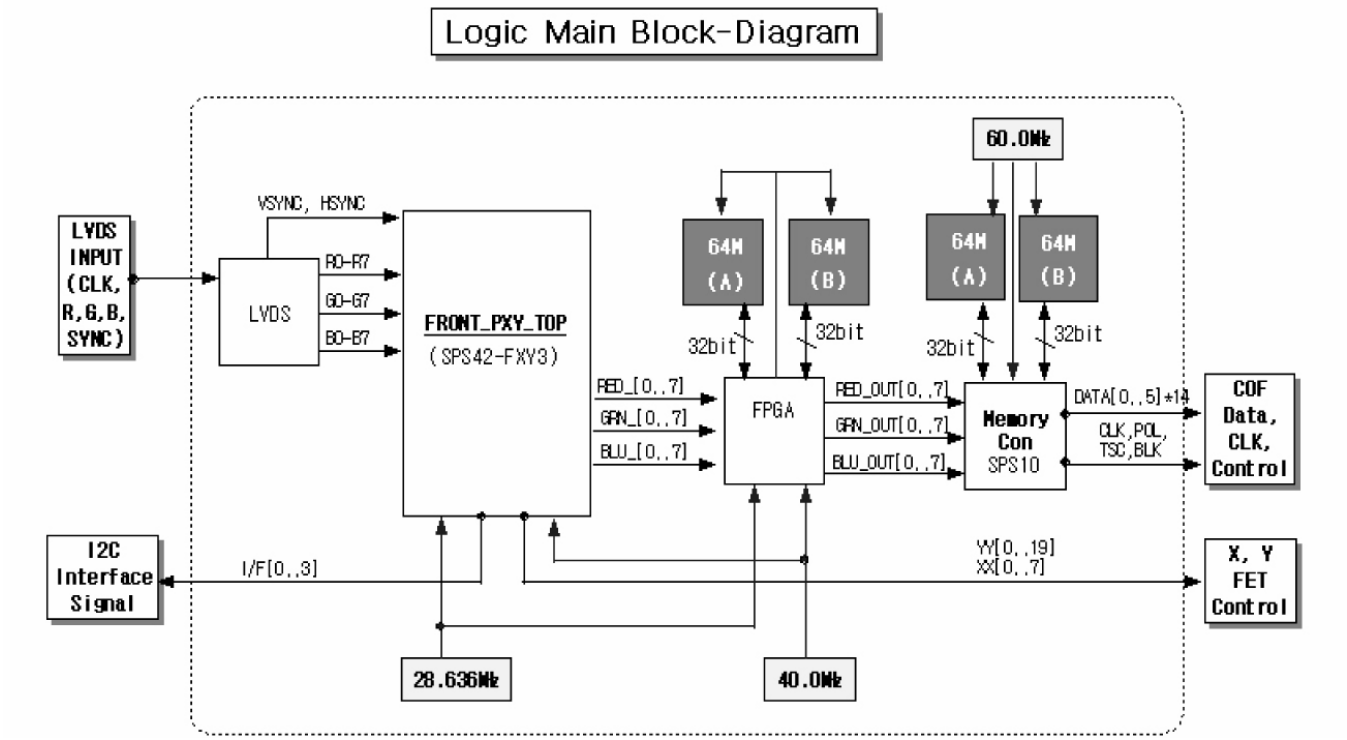
42" SDv2



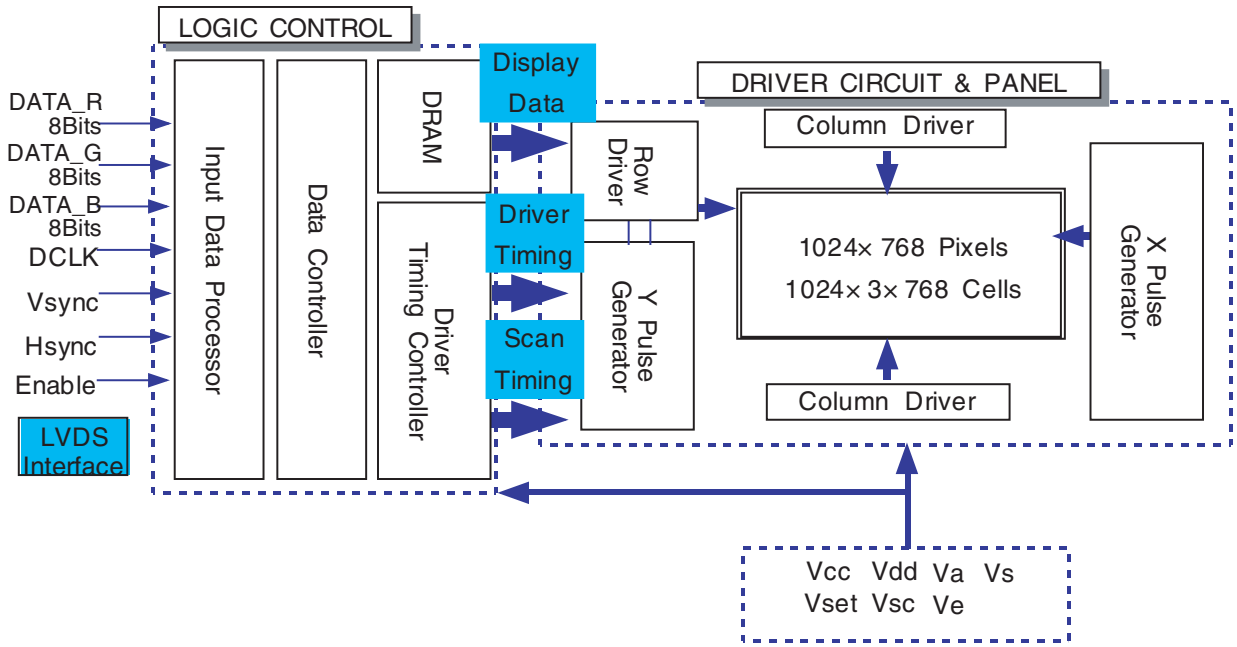
Reference

- V3.3 : Voltage for LOGIC Control
- V5 : Voltage for COF driver
- Vdd : Voltage for FET driver
- Va : Voltage for address pulse
- Vs : Voltage for sustain driver
- Vsc : Voltage for scan pulse
- Ve : Voltage for X ramppulse
- Vset : Voltage for Y ramppulse

42" SDv3



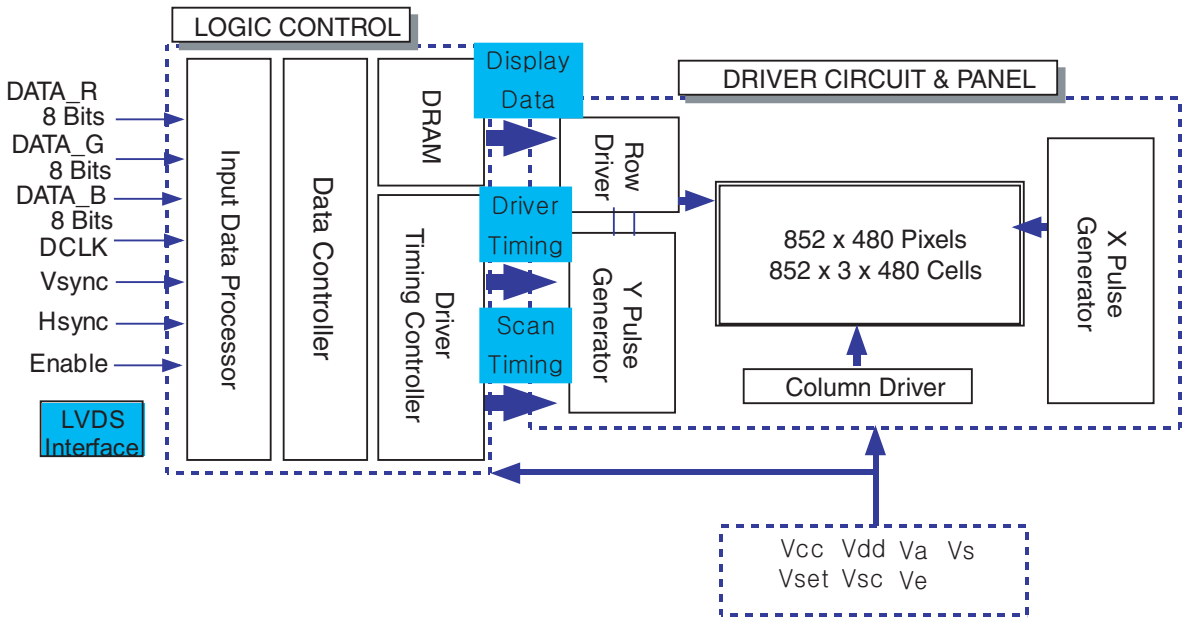
42" HDv3



Reference

- Vcc : Voltage for Logic Control
- Vdd : Voltage for Fet driver
- Va : Voltage for address pulse
- Vs : Voltage sustain pulse
- Vsc : Voltage for scan pulse
- Ve : Voltage for X ramp pulse
- Vset : Voltage for Y ramp pulse

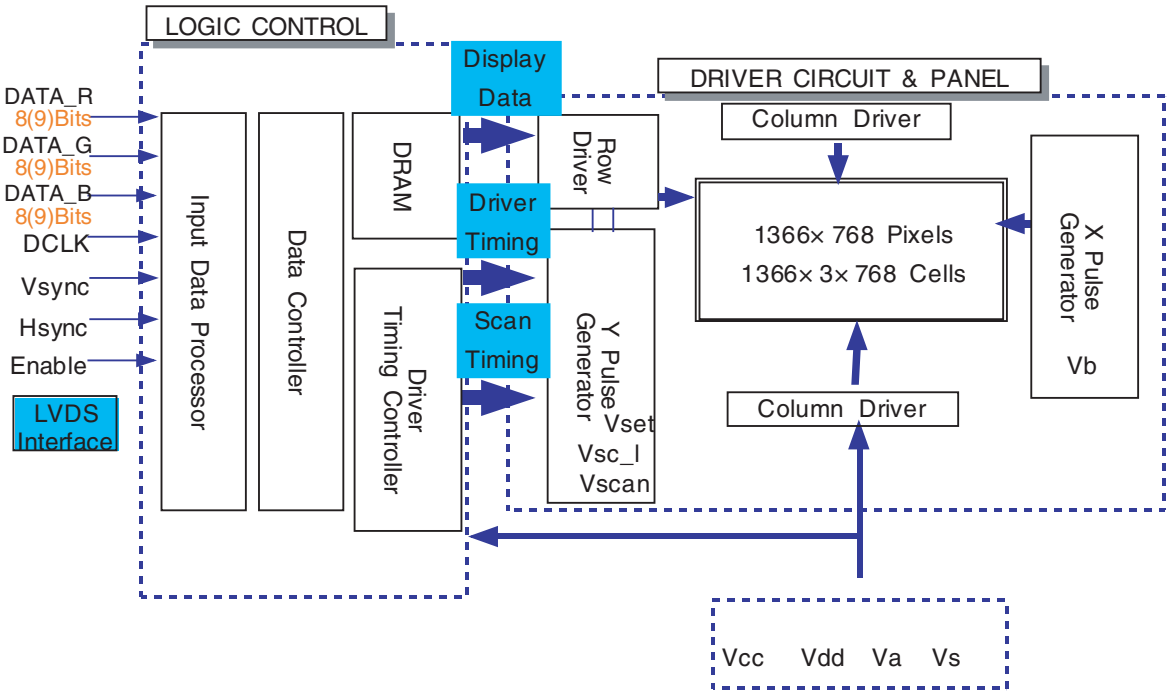
S37" SDv4



Reference

- Vcc : Voltage for Logic Control
- Vdd : Voltage for FET driver
- Va : Voltage for address pulse
- Vs : Voltage sustain pulse
- Vsc : Voltage for scan pulse
- Ve : Voltage for X ramp pulse
- Vset : Voltage for Y ramp pulse

50" HDv3

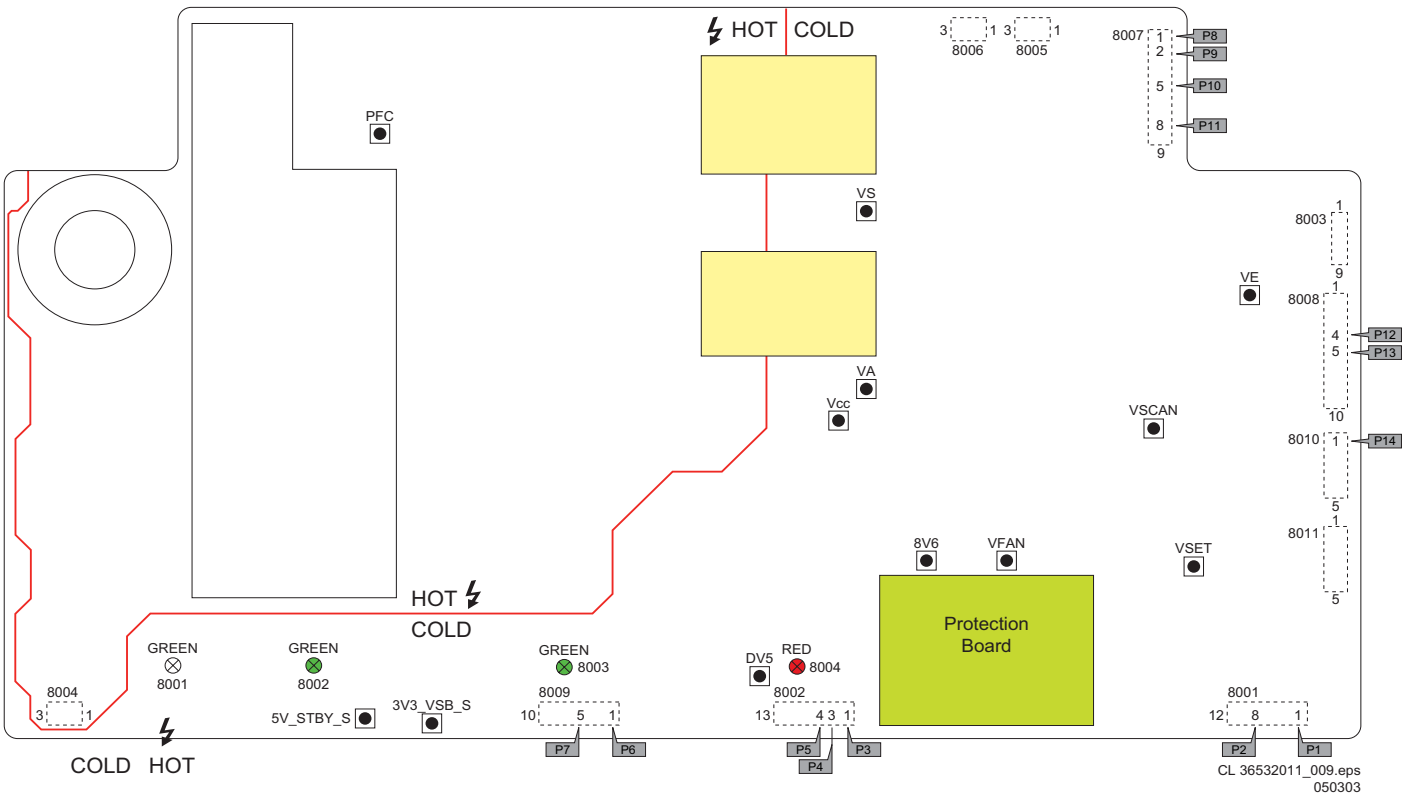


Reference

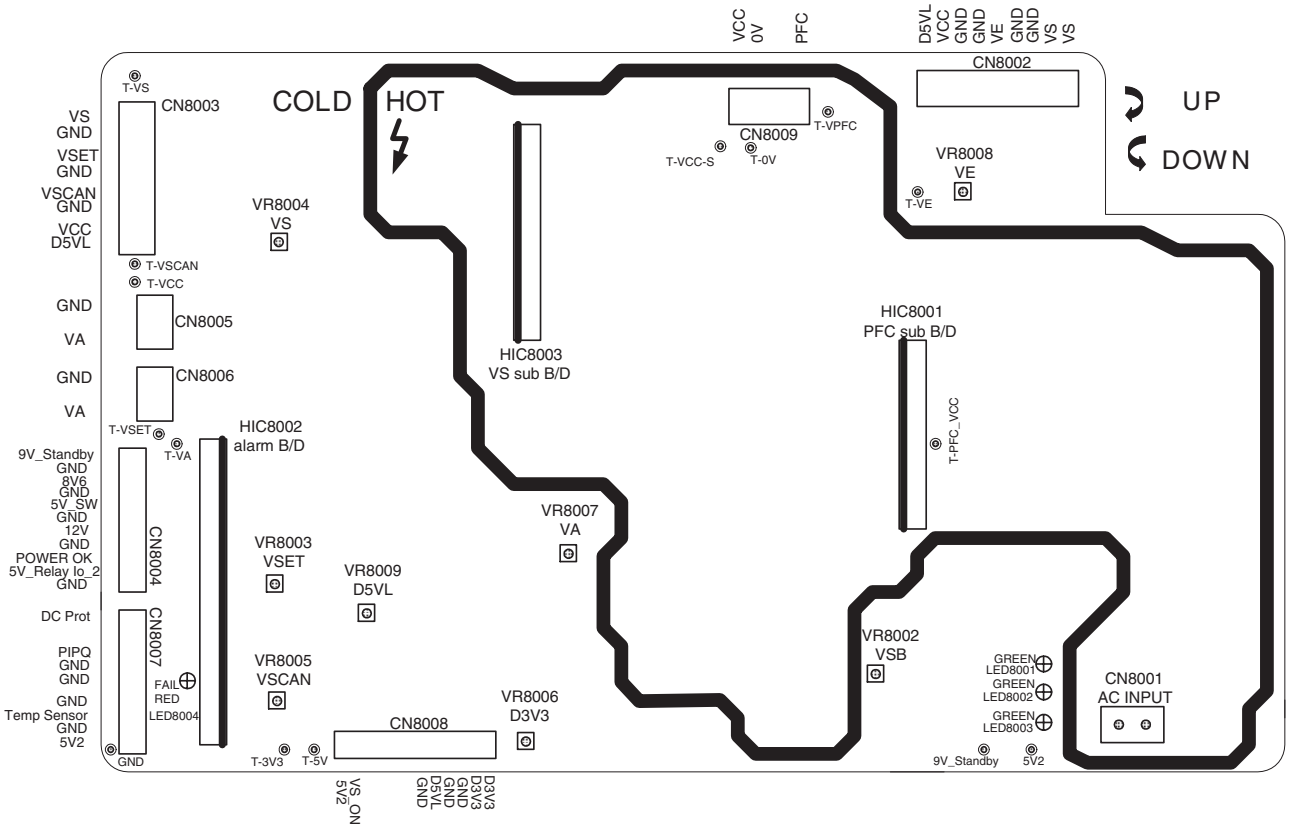
- Vcc : Voltage for Logic Control
- Vdd : Voltage for FET driver
- Va : Voltage for address pulse
- Vsc_l : Voltage sustain low
- Vscan : Voltage for scan high
- Vb : Voltage for X bias
- Vset : Voltage for Y ramp pulse

6.2 PSU Board diagram

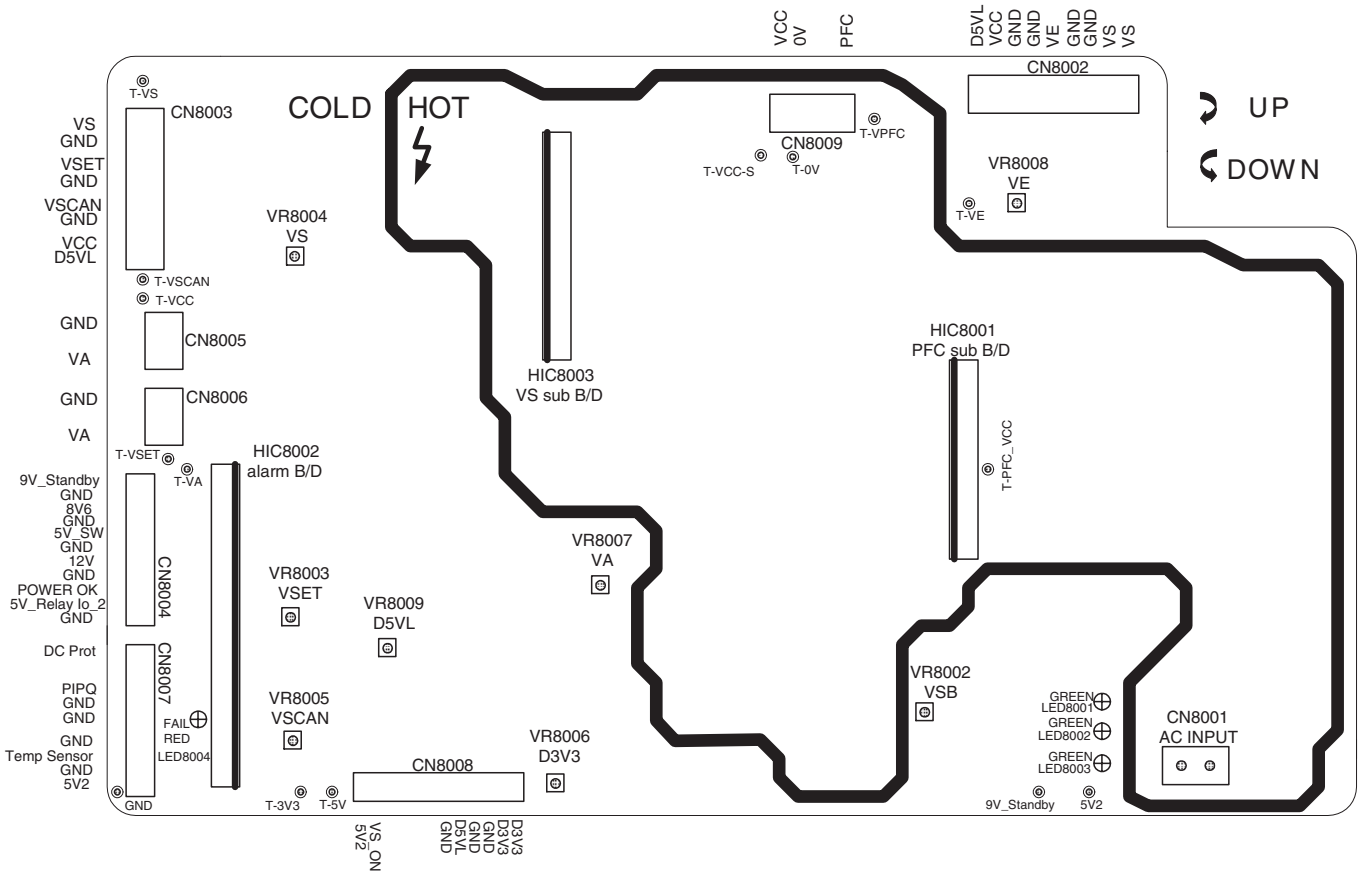
42" SDv2



42" SDv3

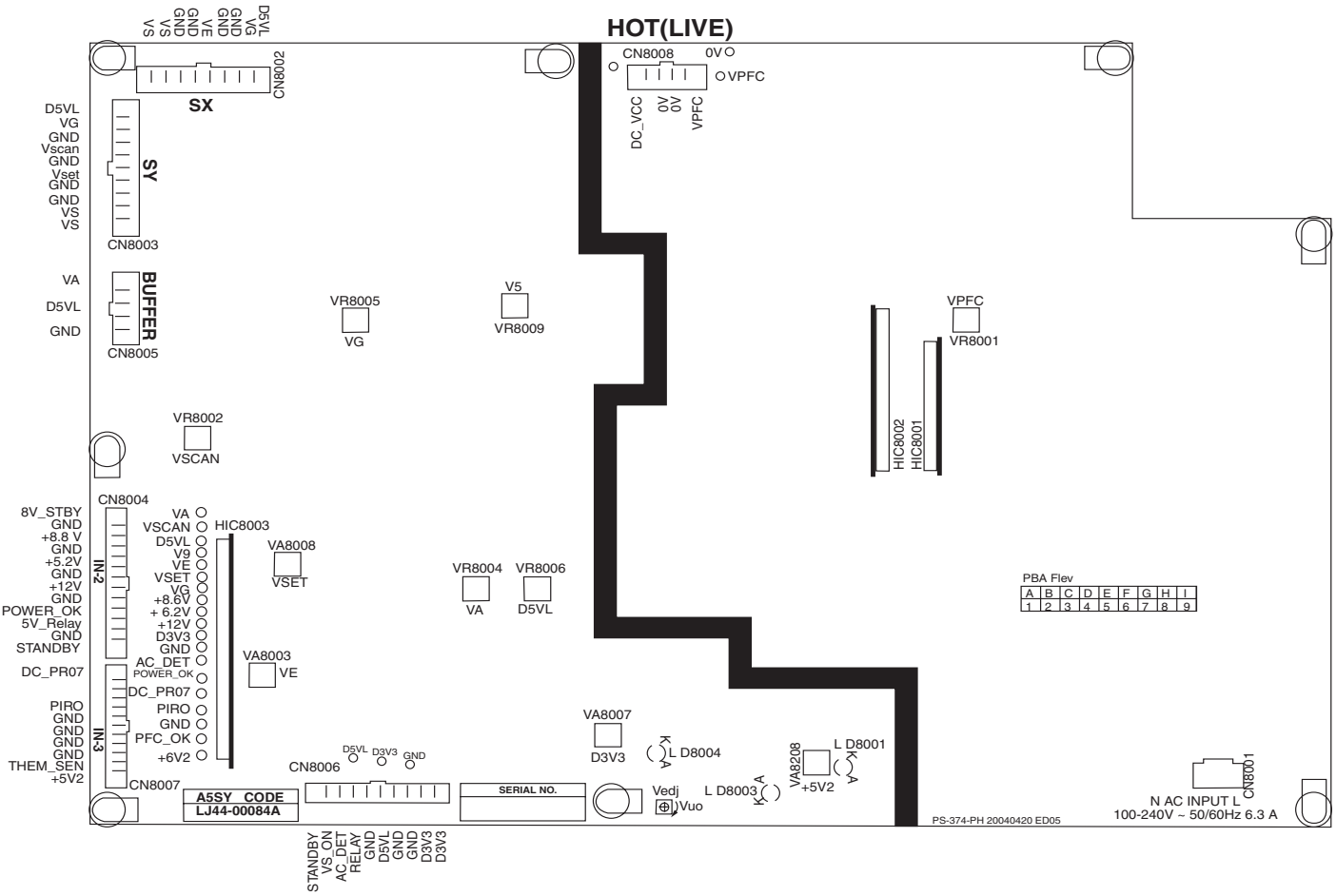


42" HDv3



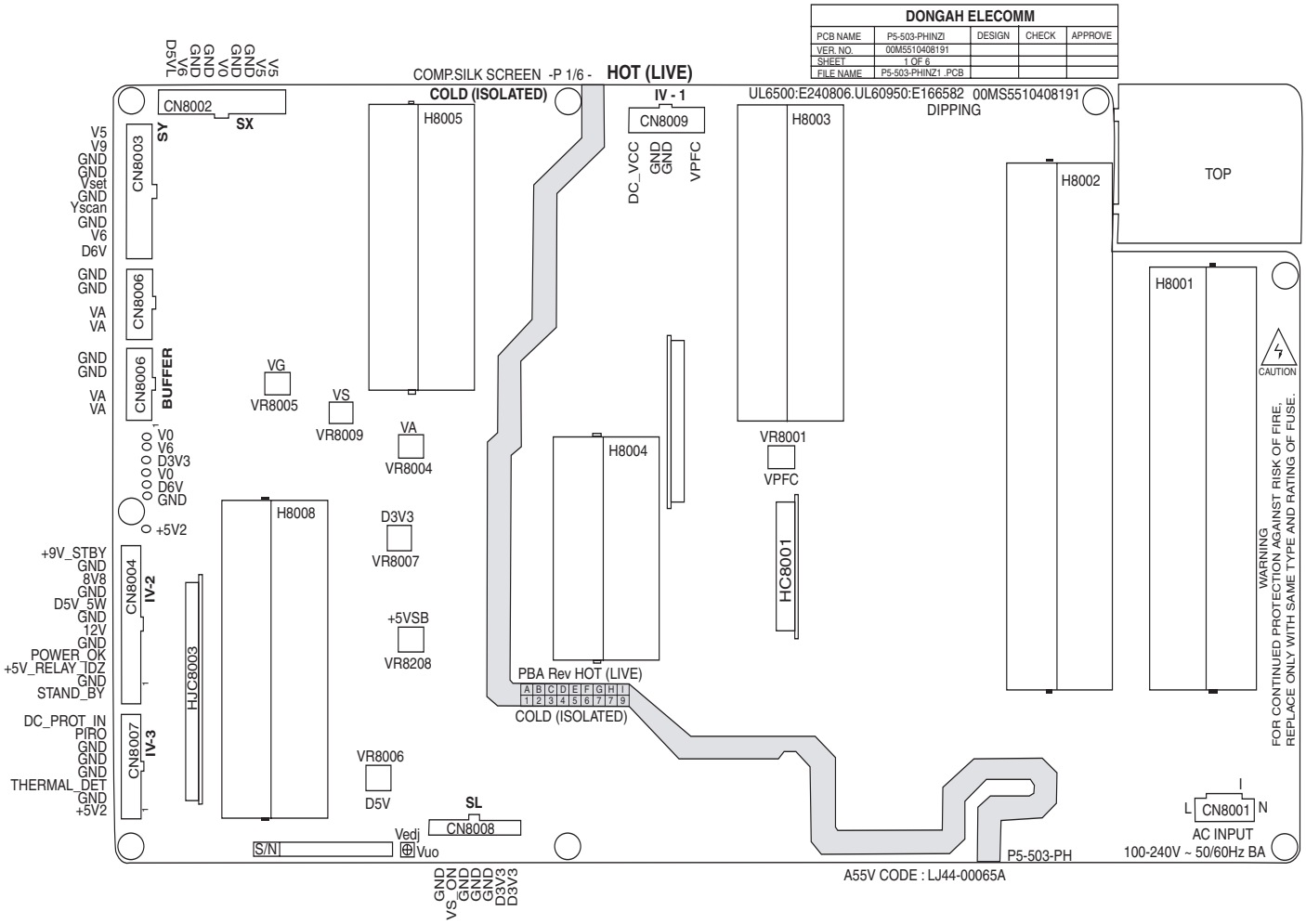
No	Output voltage(V)	Voltage Setting (Nominal Load λ)	Output Voltage Variable Point
1	PFC	Check voltage label on the PDP for correct values.	370V ~ 400V
2	VS		160V ~ 185V
3	VA		65V ~ 80V
4	VE		150V ~ 170V
5	VSET		160V ~ 180V
6	VSCAN		-55V ~ -75V
7	D5VL		4.0V ~ 6.0V
8	D3V3		2.8V ~ 4.0V
9	VCC		Fixed
10	5V2		3.5V ~ 6.0V
11	9V_Standby		Fixed

S37" SDv4



No	Output voltage(V)	Voltage Setting (Nominal Load λ)	Output Voltage Variable Point
2	VS	Check voltage label on the PDP for correct values.	160V ~ 185V
3	VA		60V ~ 80V
4	VE		165V ~ 195V
5	VSET		160V ~ 180V
6	VSCAN		-145V ~ -175V
7	D5VL		5.0V ~ 6.0V
8	D3V3		2.8V ~ 3.8V
9	VCC		Fixed
10	5V2		4.5V ~ 5.6V
11	9V_Standby		Fixed

50" HDv3



No	Output voltage(V)	Voltage Setting (Nominal Load λ)	Output Voltage Variable Point
1	PFC	Check voltage label on the PDP for correct values.	370V ~ 400V
2	VS		160V ~ 185V
3	VA		65V ~ 80V
4	VE		150V ~ 170V
5	VSET		160V ~ 180V
6	VSCAN		-55V ~ -75V
7	D5VL		4.0V ~ 6.0V
8	D3V3		2.8V ~ 4.0V
9	VCC		Fixed
10	5V2		3.5V ~ 6.0V
11	9V_Standby		Fixed

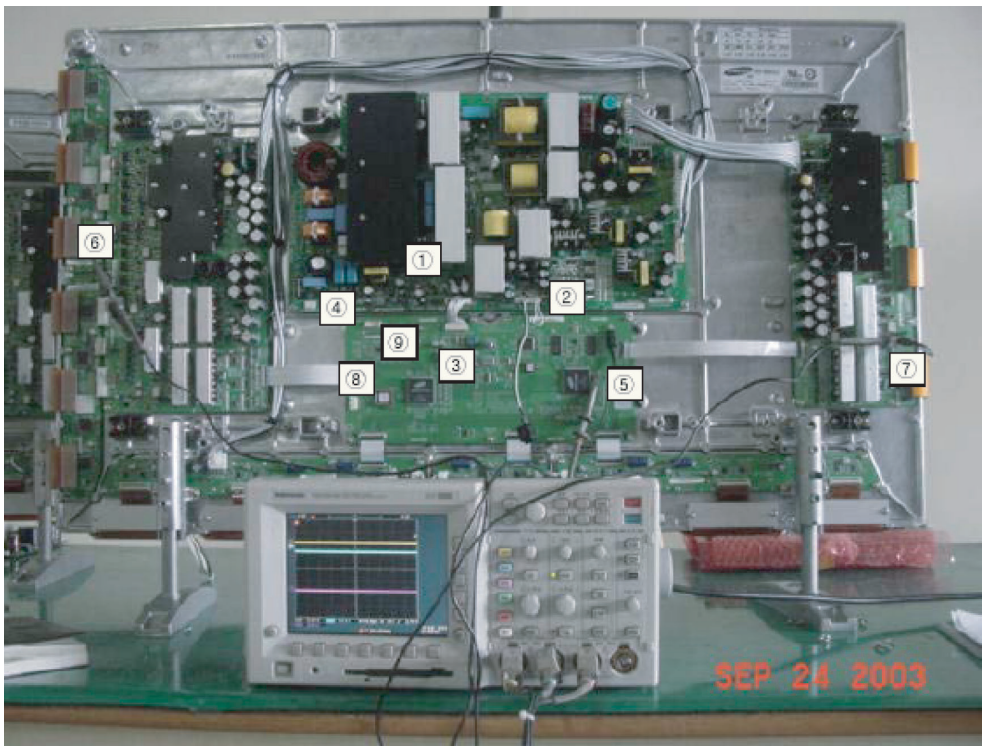
7. Circuit Diagrams and PWB Layouts

Not aplicable.

8. Aligments

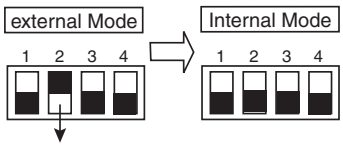
8.1 Adjustment Specification, Checking Position etc.

8.1.1 42" SDv2



1) Preparation

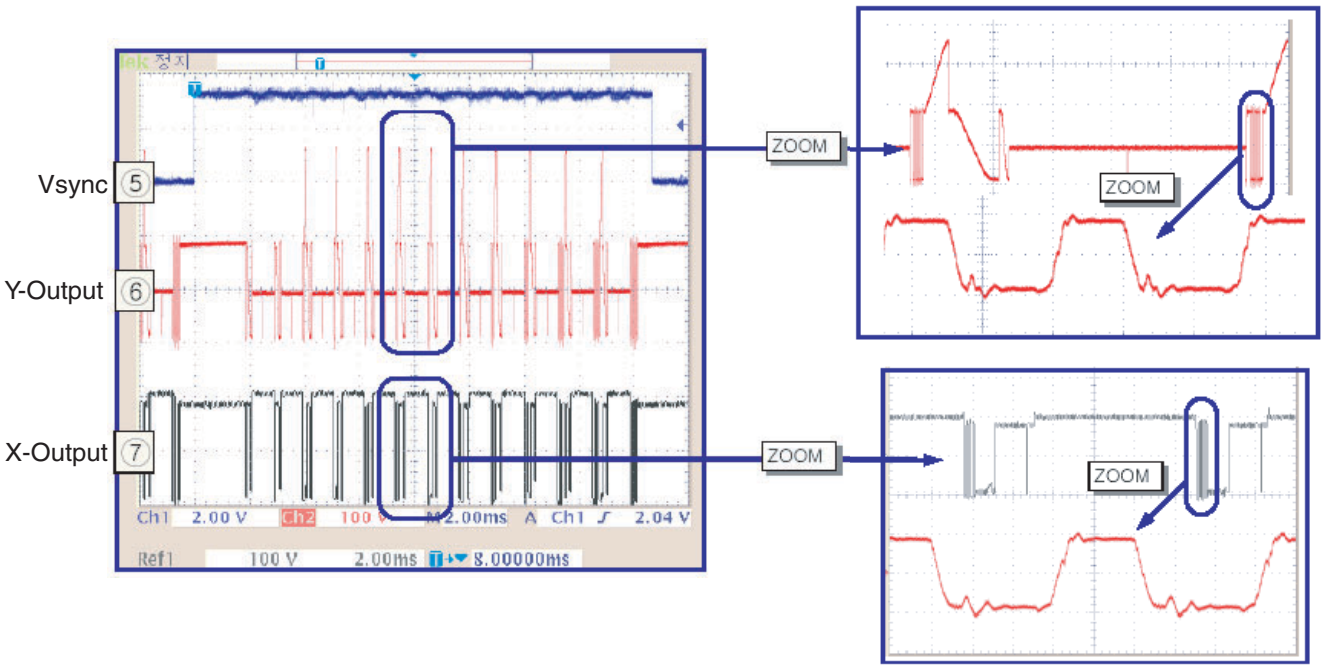
① Insert Short Bar (J8002) in SMPS
② Connect Relay Jig S/W JIG
③ Change Logic B'd S/W into internal mode



④ Insert Jig AC socket
※Oscilloscope
⑤ CH1: V-SYNC (CN201)
⑥ CH2: Y-output (OUT4)
⑦ CH3: X-output (TP OUT)
⑧ Connect Key-scan B'd

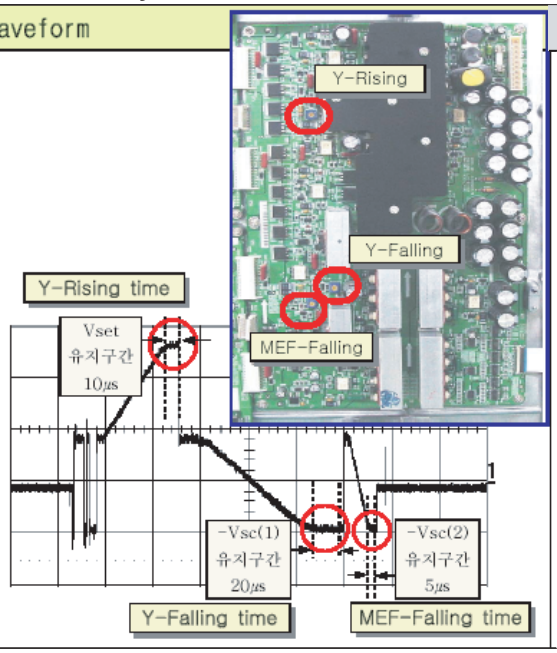
2) Turn-On.

- Turn on Power S/W
- Check LED in Logic B'd (⑨)
- Check waveform of X-B'd nad Y-B'd (Refer to Picture 1)



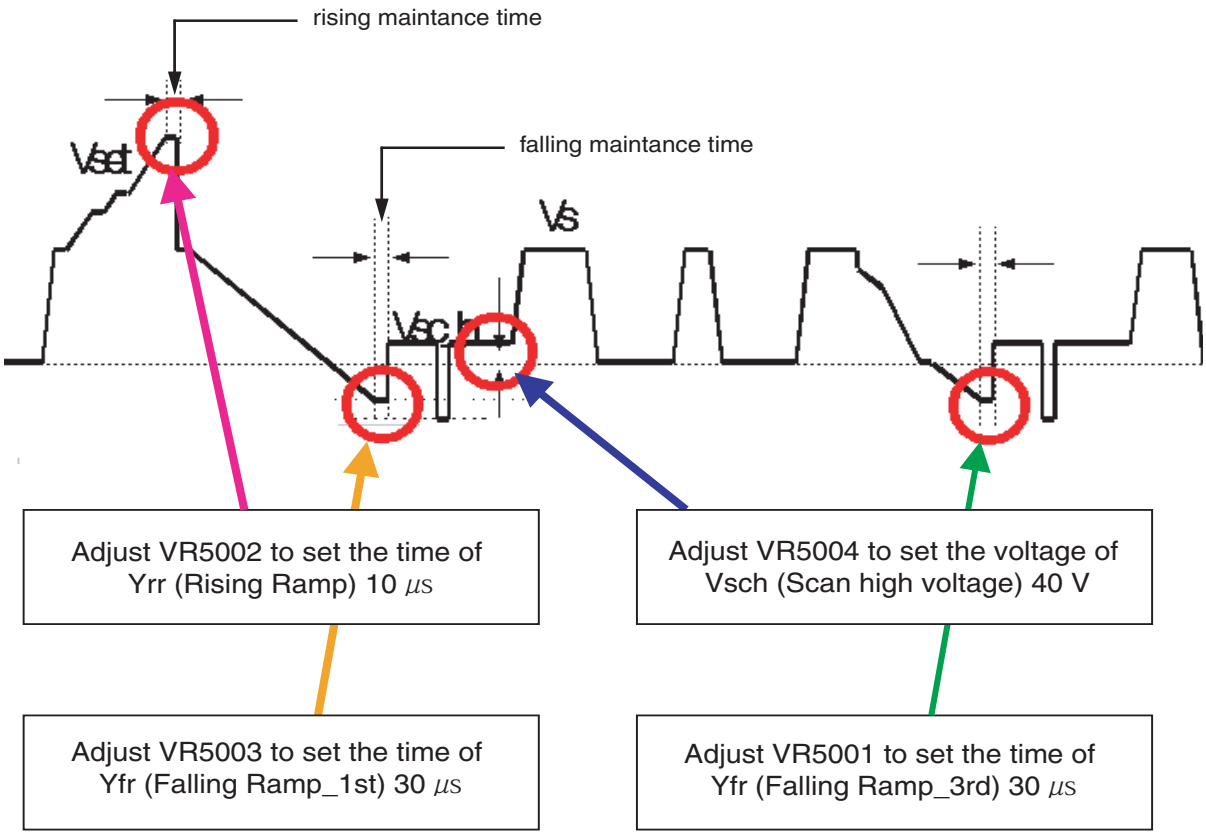
[Picture 1] Waveform of X-Board, Y-Board

How to adjust waveform

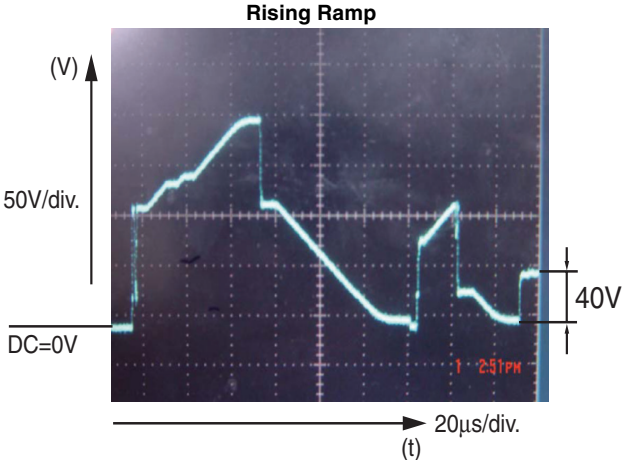
Waveform	Procedure
	1) Make Full White on Screen. 2) Observe waveform using Oscilloscope. ① check OUT4 TP in Y-buffer(upper). Observe the waveform of the third waveform of 1TV-Field. ② Adjust the division of oscilloscope like the left picture ③ Adjust the period of Vset as 10μS, that of -Vsc(1) as 20μs, that of -Vsc(2) as 5μs, turning VR (Variable Resistor) (only,when you adjust each period of -Vsc(1) & -Vsc(2) adjust Vertical Division of oscilloscope as '2V or 5V') ④ VR for Vset : VR5003 (Y_main) VR for -Vsc(1) : VR5001 (Y_main) VR for -Vsc(2) : VR5002 (Y_main)

8.1.2 42" SDv3

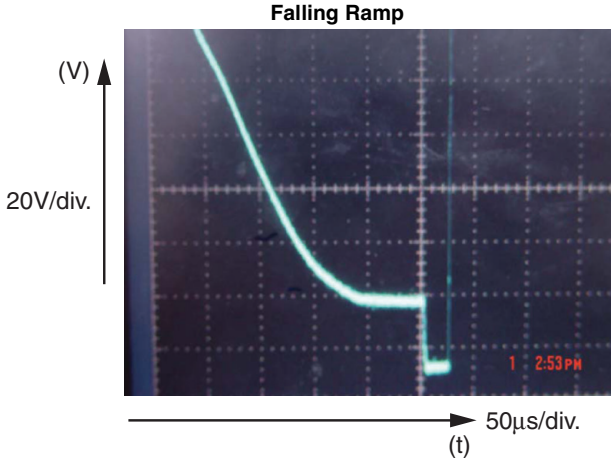
V3.1 TCP Ramp Waveform Inclination Adjustment (Y-Board)

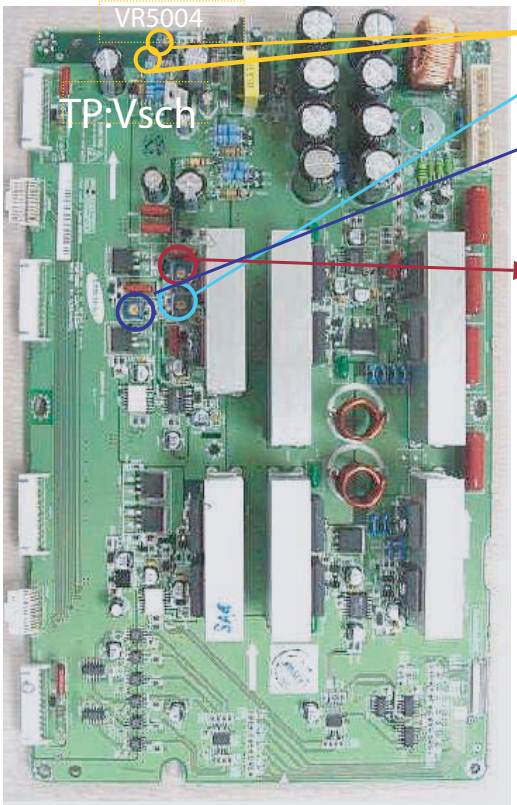

rising maintance time
falling maintance time
Vset
Vs
Vsch
Adjust VR5002 to set the time of Yrr (Rising Ramp) 10 μs
Adjust VR5004 to set the voltage of Vsch (Scan high voltage) 40 V
Adjust VR5003 to set the time of Yfr (Falling Ramp_1st) 30 μs
Adjust VR5001 to set the time of Yfr (Falling Ramp_3rd) 30 μs

Rising Ramp



Falling Ramp



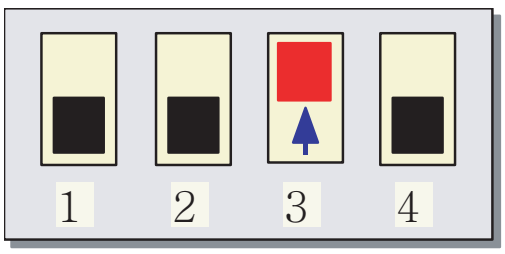


1. VR5004 Adjustment: Vsch TP => 40volt
2. VR5002 Adjustment: Rising Ramp flat time: Typ. 10 µsec
3. VR5003 Adjustment: Falling Ramp flat time => Typ. 30 µsec
4. VR5001 Adjustment: 3th SF Falling Ramp flat time => Typ. 30 µsec

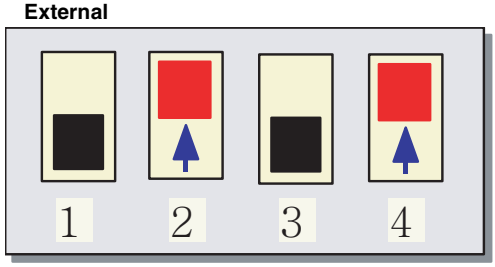
* Pay close attention to above adjustment

*** Dip Switch Mode**

Internal

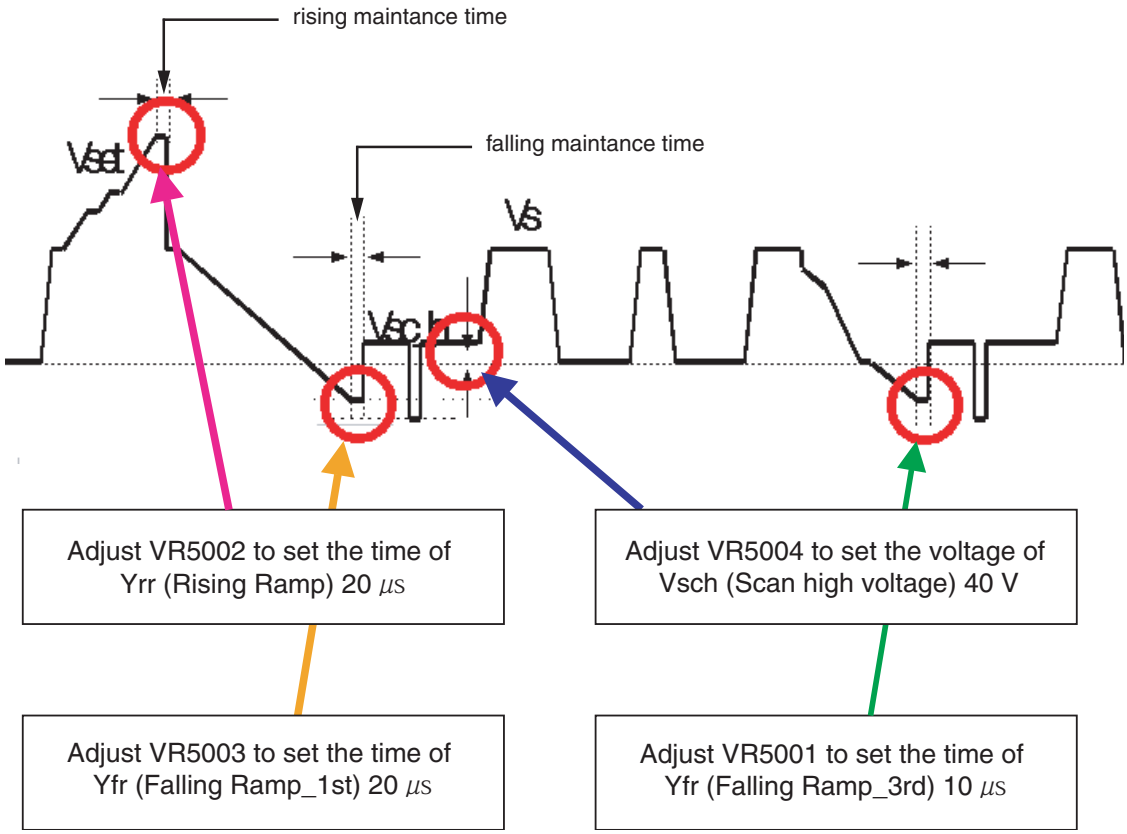


External

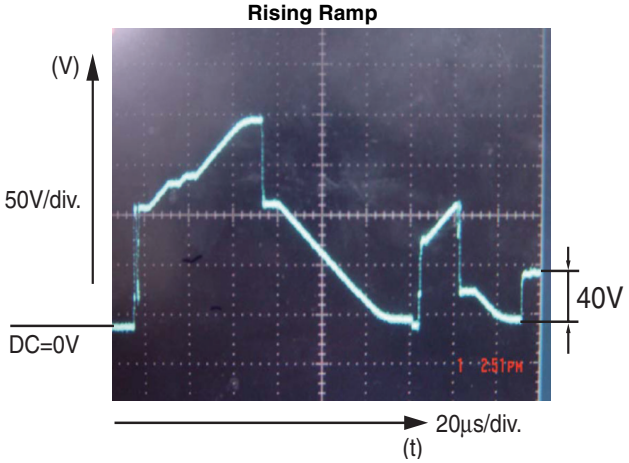


8.1.3 42" HDv3

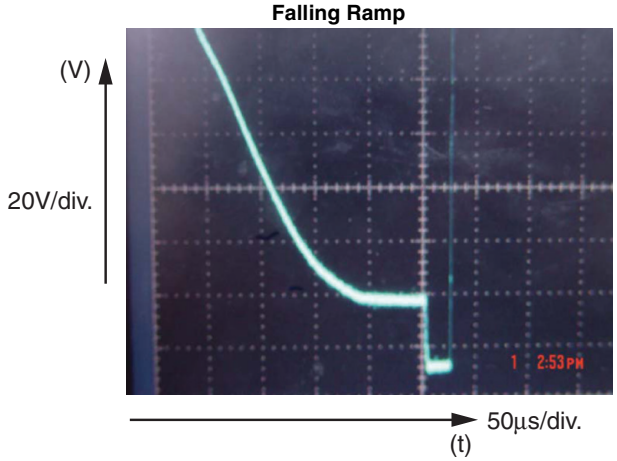
V3.1 TCP Ramp Waveform Inclination Adjustment (Y-Board)

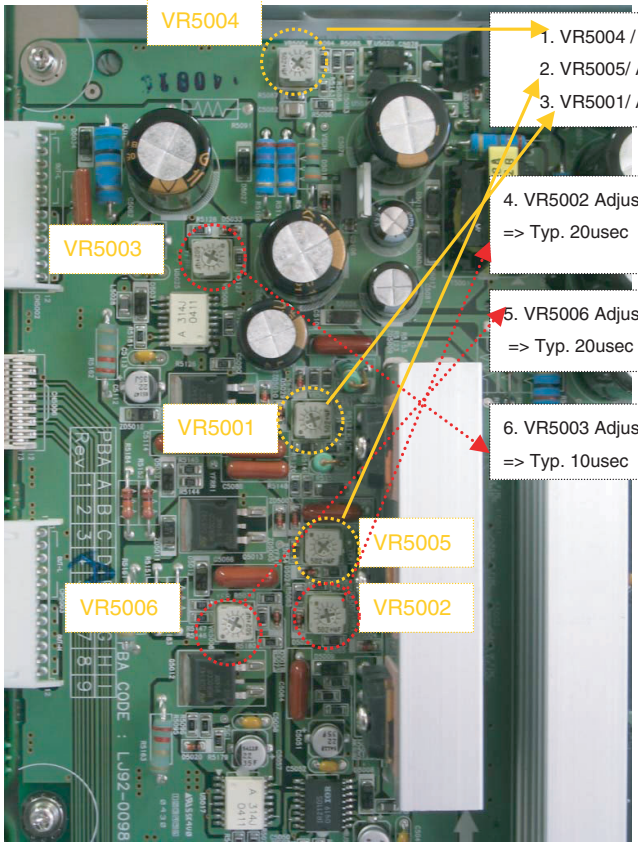

rising maintance time
falling maintance time
Vset
Vs
Vsch
Adjust VR5002 to set the time of Yrr (Rising Ramp) 20 μs
Adjust VR5004 to set the voltage of Vsch (Scan high voltage) 40 V
Adjust VR5003 to set the time of Yfr (Falling Ramp_1st) 20 μs
Adjust VR5001 to set the time of Yfr (Falling Ramp_3rd) 10 μs

Rising Ramp



Falling Ramp





1. VR5004 / Adjustment; Clock-wise to max
2. VR5005/ Adiustment; Clock-wise to max
3. VR5001/ Adiustment; Clock-wise to 4 th division

4. VR5002 Adjustment: Rising Ramp flat time:
=> Typ. 20usec

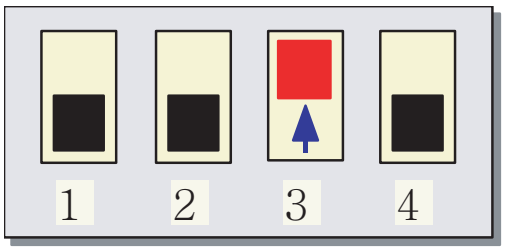
5. VR5006 Adjustment: Falling Ramp flat time
=> Typ. 20usec

6. VR5003 Adjustment: 3th SF Falling Ramp flat time
=> Typ. 10usec

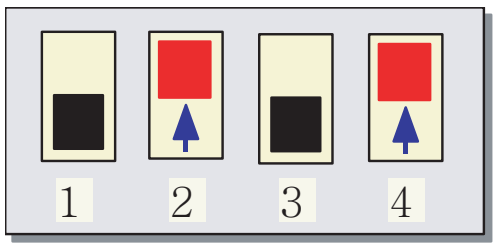
* Pay close attention to above adjustment

*** Dip Switch Mode**

Internal

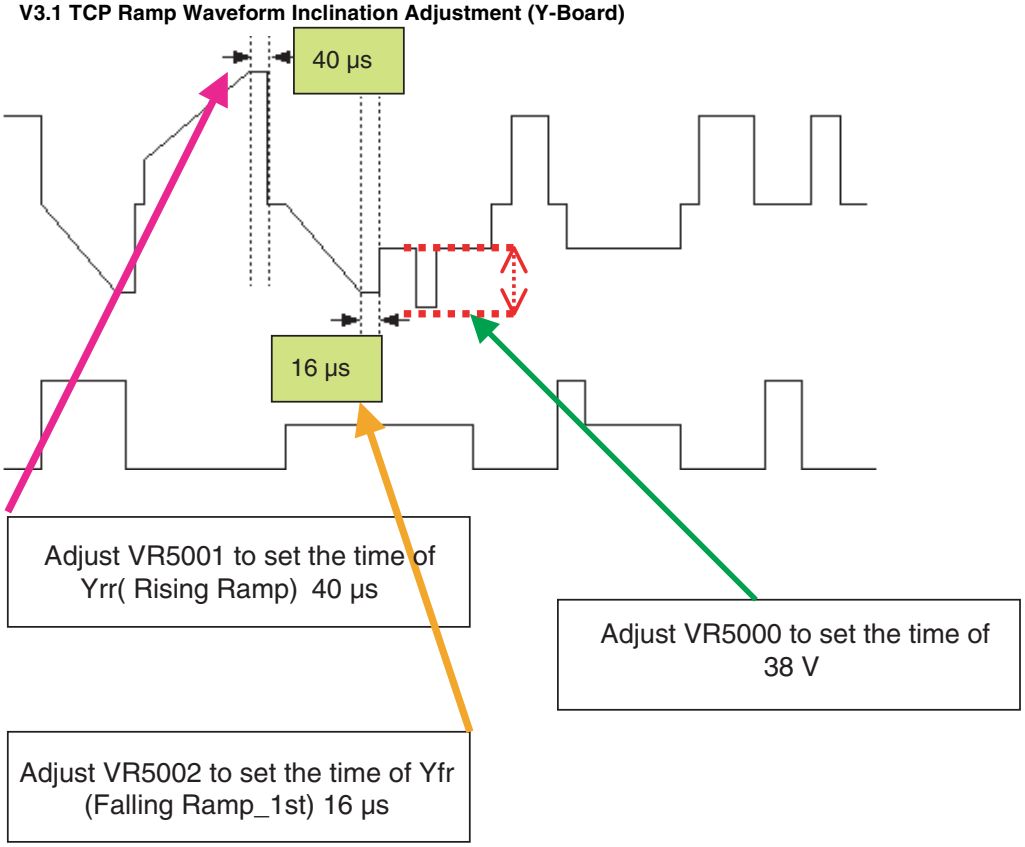


External

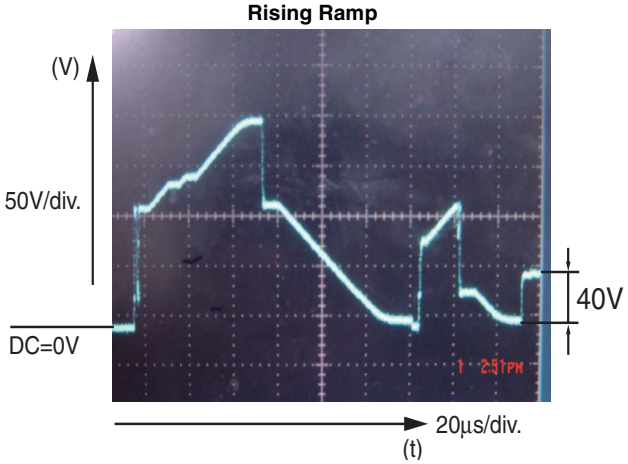


8.1.4 S37" SDv4

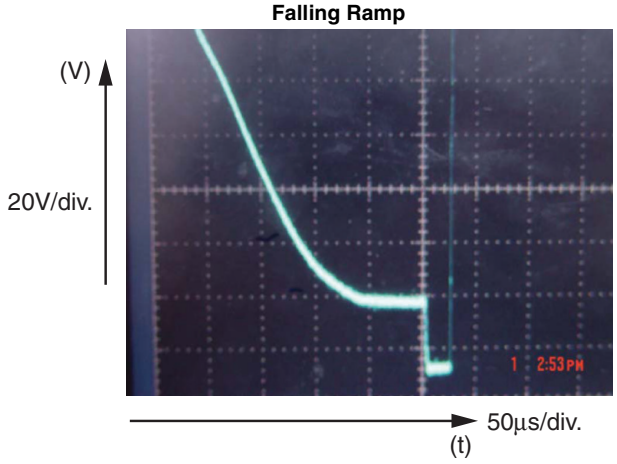
V3.1 TCP Ramp Waveform Inclination Adjustment (Y-Board)

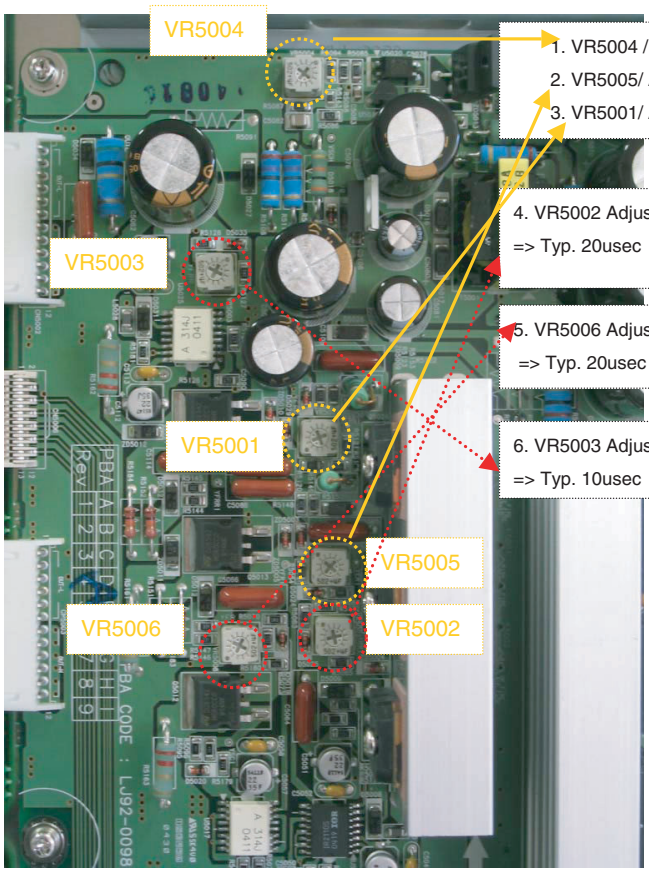

40 µs
16 µs
Adjust VR5001 to set the time of Yrr(Rising Ramp) 40 µs
Adjust VR5000 to set the time of 38 V
Adjust VR5002 to set the time of Yfr (Falling Ramp_1st) 16 µs

Rising Ramp



Falling Ramp





1. VR5004 / Adjustment; Clock-wise to max
2. VR5005/ Adiustment; Clock-wise to max
3. VR5001/ Adiustment; Clock-wise to 4 th division

4. VR5002 Adjustment: Rising Ramp flat time:
=> Typ. 20usec

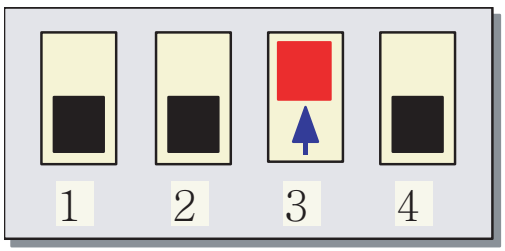
5. VR5006 Adjustment: Falling Ramp flat time
=> Typ. 20usec

6. VR5003 Adjustment: 3th SF Falling Ramp flat time
=> Typ. 10usec

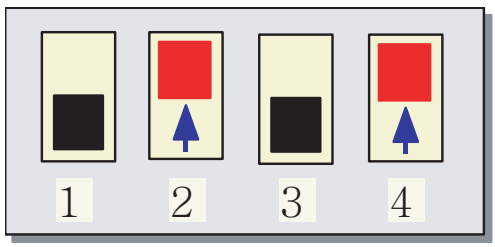
* Pay close attention to above adjustment

*** Dip Switch Mode**

Internal

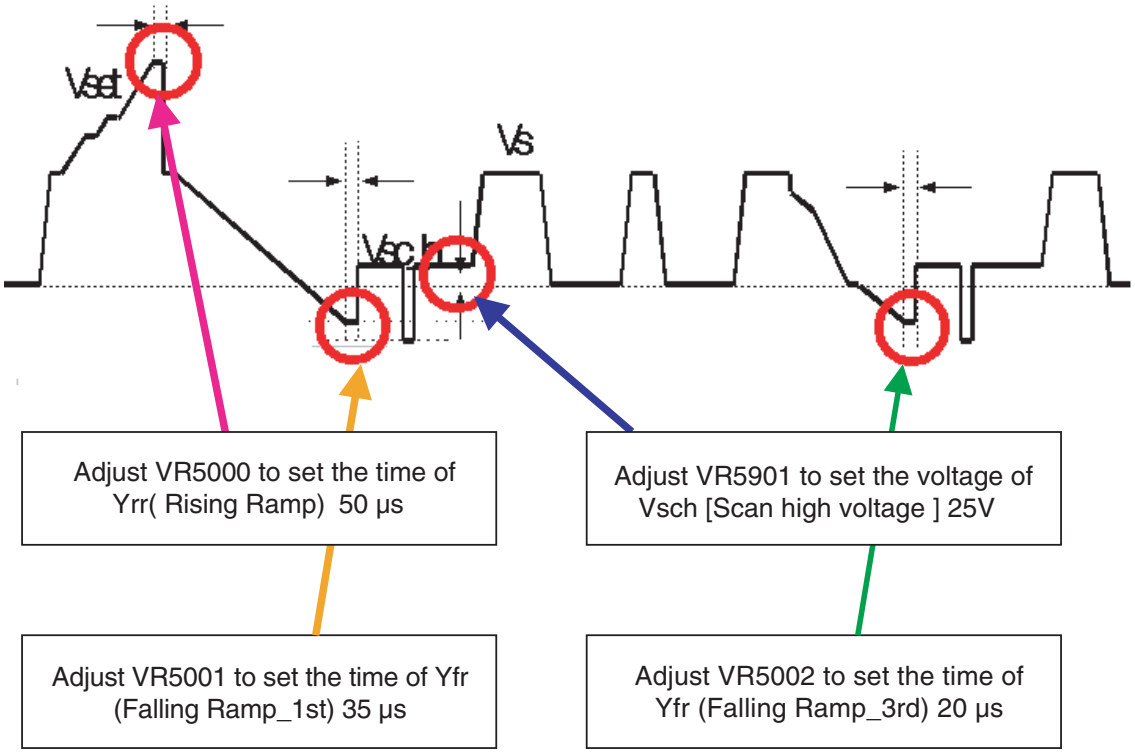


External

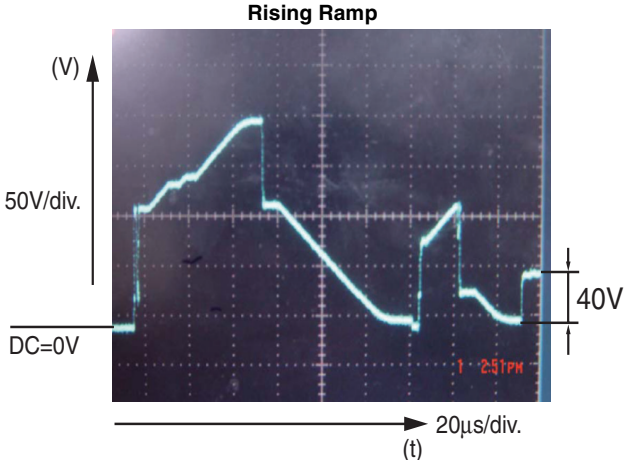


8.1.5 50" HDv3

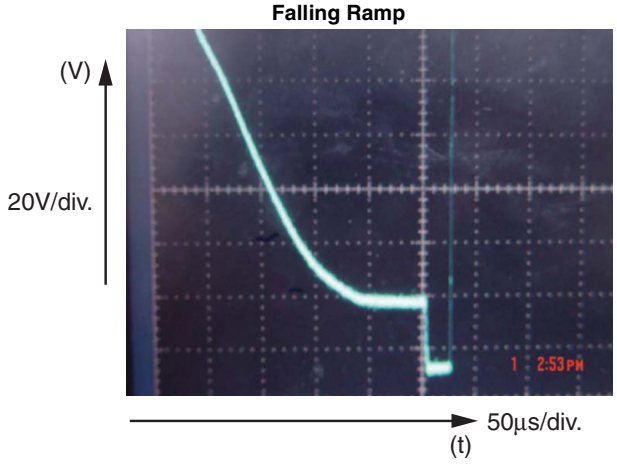
V3.1 TCP Ramp Waveform Inclination Adjustment (Y-Board)

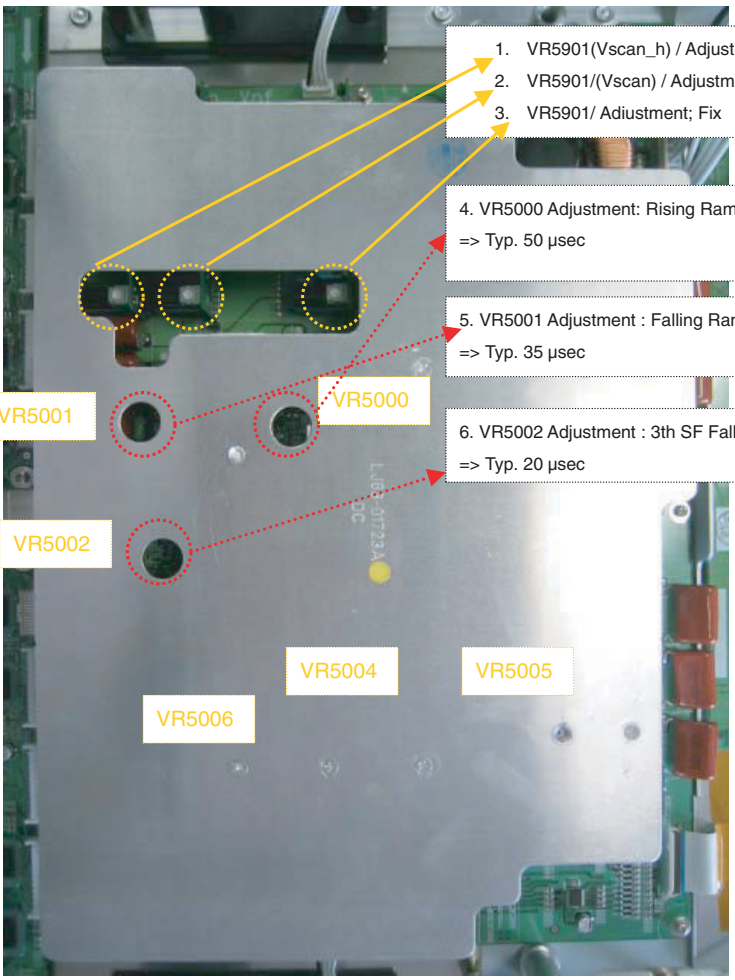

Vset
Vs
Vsch
Adjust VR5000 to set the time of Yrr(Rising Ramp) 50 µs
Adjust VR5901 to set the voltage of Vsch [Scan high voltage] 25V
Adjust VR5001 to set the time of Yfr (Falling Ramp_1st) 35 µs
Adjust VR5002 to set the time of Yfr (Falling Ramp_3rd) 20 µs

Rising Ramp



Falling Ramp

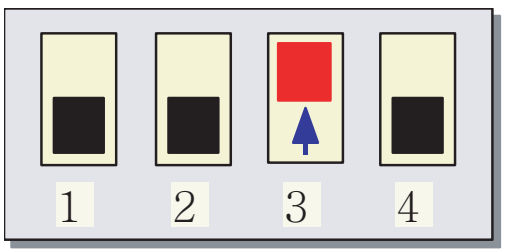




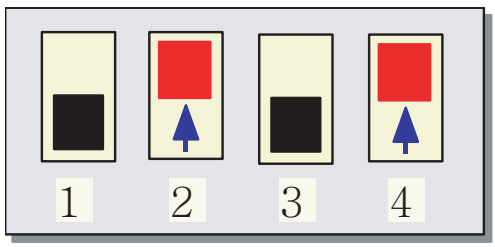
* Pay close attention to above adjustment

*** Dip Switch Mode**

Internal



External



8.2 Adjusting procedure

42" SDv3 (SDv2)
1. Get Pattern to be Full White.
2. Adjust Vsch to 40V with VR5004.
3. Check the waveform with an Oscilloscope.
   - Triggering through V-sync of LOGIC Board.
   - Connect the OUT 4 Test Point at the center of Y_buffer to other channel, and then check the first SF operating waveform of 1TV-Field.
   - Check the waveform as before by adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
   - Set the Vset to 10μsby adjusting VR5002.
   - Set the Falling maintenance time to 30μs by adjusting R5003.
   - Change the waveform position of Oscilloscope to 3SF and then set the Falling maintenance time to 30μsby adjusting the VR5001. GND maintenance section should be checked after the Vertical Division is readjusted to '2V or 5V'.

Special Notice: When you adjust the inclination of waveform, do check and adjustment being based on the Reset waveform of 1st Sub-field of 1st Frame and then move to 3rd Sub-field for adjusting.

42" HDv3
1. Get Pattern to be Full White.
2. Adjust Vsch to Clock-wise max by using VR5004 (Vsch should be connected to "+" unit of DMM).
3. Check the waveform using Oscilloscope.
   - Triggering through V_TOGG of LOGIC Board.
   - Connect the OUT 4 Test Point at the center of Y_buffer to other channel, and then check the first SF operating waveform of 1TV-Field.
   - Check the waveform as before by adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
   - Set the Vset to 20μs by adjusting VR5002. GND maintenance section should be checked after the Vertical Division is readjusted to '2V or 5V'.
   - Set the Falling maintenance time to 20μs by adjusting R5006.
   - Change the waveform position of Oscilloscope to 3SF and then set the Falling maintenance time to 10μs by adjusting the VR5003. GND maintenance section should be checked after the Vertical Division is readjusted to '2V or 5V'.

Special Notice: When you adjust the inclination of waveform, do check and adjustment being based on the Reset waveform of 1st Sub-field of 1st Frame and then move to 3rd Sub-field for adjusting.

S37" SDv4
1. Get Pattern to be Full White.
2. Adjust Vsch to 40V by using VR5004 (Vsch should be connected to "+" unit of DMM). Vsch is over 95V than Vsc_l.
3. Check the waveform using Oscilloscope.
   - Triggering through V_TOGG of LOGIC Board.
   - Connect the OUT 4 Test Point at the center of Y_buffer to other channel, and then check the first SF operating waveform of 1TV-Field.
   - Check the waveform as before by adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
   - Set the Vset to 40μs by adjusting VR5001. GND maintenance section should be checked after the Vertical Division is readjusted to '2V or 5V'.
   - Set the Falling maintenance time to 16μs by adjusting R5002.
   - Change the waveform voltage GND to 38V by adjusting the VR5000.

Special Notice: When you adjust the inclination of waveform, do check and adjustment being based on the Reset waveform of 1st Sub-field of 1st Frame and then move to 3rd Sub-field for adjusting.

50" HDv3
1. Get Pattern to be Full White.
2. Adjust Vsch to 25V by using VR5901_VSC_h (Vsc_h should be connected to "+" unit of DMM).
3. Check the waveform using Oscilloscope.
   - Triggering through V_TOGG of LOGIC Board.
   - Connect the OUT 4 Test Point at the center of Y_buffer to other channel, and then check the first SF operating waveform of 1TV-Field.
   - Check the waveform as before by adjusting Horizontal Division. Check the Reset waveform when the V_TOGG Level is changed.
   - Set the Rising Ramp Flat Time to 50μs by adjusting VR5000. GND maintenance section should be checked after the Vertical Division is readjusted to '2V or 5V'.
   - Set the Falling maintenance time to 35μs by adjusting R5001.
   - Change the waveform position of Oscilloscope to 3SF and then set the Falling maintenance time to 20μs by adjusting the VR5002.
   - GND maintenance section should be checked after the Vertical Division is readjusted to '2V or 5V'.

Special Notice: When you adjust the inclination of waveform, do check and adjustment being based on the Reset waveform of 1st Sub-field of 1st Frame and then move to 3rd Sub-field for adjusting.

Alignment table Y PWB

	Wave Form	Adjusting Location No	Default
37SDV4	Rising_Ramp	VR5001	30 μs (30 ~ 40)
	Falling_Ramp_1st	VR5002	16 μs (10 ~ 20)
	Vsch	VR5000	38V
42SDV2	Rising_Ramp (Vset)	VR5003	10 μs
	-Vsc 1	VR5001	20 μs
	-Vsc 2	VR5002	5 μs
42SDV3	Rising_Ramp	VR5002	10 μs
	Falling_Ramp_1st	VR5003	30 μs
	Falling_Ramp_3rd	VR5001	30 μs
	Vsch	VR5004	40V
42HDV3	Rising_Ramp	VR5002	10 μs
	Falling_Ramp_1st	VR5003	20 μs
	Falling_Ramp_3rd	VR5001	10 μs
	Vsch Scan high voltage	VR5004	40V
50HDV3	Rising_Ramp	VR5000	50 μs
	Falling_Ramp_1st	VR5001	35 μs
	Falling_Ramp_3rd	VR5002	20 μs
	Vsch Scan high voltage	VR5901	25V

9. Circuit Descriptions

9.1 Main function of Each Assembly

9.1.1 X-main board

The X-main board generate a drive signal by switching the FET in synchronization with logic
main board timing and supplies the X electrode of the panel with the drive signal through the
connector.

1. Maintain voltage waveforms (including ERC)
2. Generate X rising ramp signal
3. Maintain Ve bias between Scan intervals

9.1.2 Y-main board

The Y-main board generate a drive signal by switching the FET in synchronization with the logic
Main Board timing and sequentially supplies the Y electrode of the panel with the drive signal
through the scan driver IC on the Y-buffer board. This board connected to the panel's
Y terminal has the following main functions.

1. Maintain voltage waveforms (including ERC)
2. Generate Y-rising Falling Ramp
3. Maintain V scan bias

9.1.3 Logic main board

The logic main board generates and outputs the address drive output signal and the X ,Y drive signal by processing the video signals. This Board buffers the address dirve output signal and feeds it to the address drive IC (COF module, video signal- X Y drive signal generation , frame memory circuit / address data rearrangement).

9.1.4 Logic buffer(E,F)

The logic buffer transmits data signal and control signal.

9.1.5 Y-buffer board (Upper, Lower)

The Y-buffer board consisting of the upper and lower boards supplies the Y-terminal with scan waveforms. The board comprises 8 scan driver IC's (ST microelectronics STV 7617 : 64 or 65 output pins) , but 4 ICs for the SD class.

9.1.6 AC Noise Filter

The AC Noise filter has function for removing noise(low Frequency) and blocking surge. It effects Safety standards (EMC,EMI).

9.1.7 TCP(Tape Carrier Package)

The TCP applies Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise 4 data driver Ics(STV7610A :96 pins output pins) 7 TCPs are required for signal scan.

9.2 Abbrevitation

TCP	Tape Carrier Package
FFC	Flat Foil Cable (connection)
COF	Circuit on Foil
FPC	Flexible Printed Circuit
Vsc H or Vsc L	V Scan High or Low
SF	Sub Frame
Vset RR	Vset Raising Ramp (Flat time)
Vset FR	Vset Falling Ramp (flat time)
VR	Variable resistor
YBU & YBL	
YBM	

10. Spare Parts List

42"SDv2

PDP type

S42SD-YD06	9322 195 45682	PDP model name (non spare)
S42SD-YB04	9965 000 17797	PDP without PSU

BOARDS

LJ92-00632A	9965 000 17726	Logic-Buffer(E)
LJ92-00633A	9965 000 17725	Logic-Buffer(F)
LJ92-00634A	9965 000 17724	Logic-Buffer(G)
LJ92-00751A	9965 000 17727	Y-Buffer(up)
LJ92-00750A	9965 000 17728	Y-Buffer(down)
LJ92-00818A	9965 000 17729	Logic-Board
LJ92-00998A	9965 000 17720	X-Board
LJ92-00999A	9965 000 17731	Y-Board
LJ44-00049A	9965 000 17730	SMPS(PSU)

42"SDv3

PDP type

S42SD-YD05	9322 215 27682	PDP model name (non spare)
S42SD-YB03	9965 000 25997	PDP without PSU

BOARDS

LJ92-00811A	9965 000 25109	Logic-Buffer(E)
LJ92-00812A	9965 000 25110	Logic-Buffer(F)
LJ92-00813A	9965 000 25111	Logic-Buffer(G)
LJ92-00796A	9965 000 25112	Y-Buffer(up)
LJ92-00797A	9965 000 25113	Y-Buffer(down)
LJ92-00975D	9965 000 25114	Logic-Board
LJ92-00943A	9965 000 25115	X-Board
LJ92-00944B	9965 000 25116	Y-Board
LJ44-00058A	9965 000 25108	SMPS(PSU)
LJ44-00075A	9965 000 25131	SUB PSU

37"SDv4

PDP type

S37SD-YD02	8204 000 77261	PDP model name (non spare)
S37SD-YB01	9965 000 26018	PDP without PSU

BOARDS

LJ92-00976A	9965 000 26187	Logic-Buffer(E)
LJ92-00977A	9965 000 26188	Logic-Buffer(F)
LJ92-01002A	9965 000 26189	Logic-Buffer(G)
LG92-01022A	9965 000 26190	Y-Buffer(up)
LJ92-01056A	9965 000 26191	Logic-Board
LJ92-01020A	9965 000 26192	X-Board
LJ92-01021A	9965 000 26193	Y-Board
LJ44-00084A	9965 000 26194	SMPS(PSU)
LJ44-00075A	9965 000 25131	SUB PSU

42"HDv3 *not used in Eu sets

PDP type

S42AX-XD02	9322 215 25682	PDP model name (non spare)
S42AX-XB01	9965 000 26016	PDP without PSU

BOARDS

LJ92-00895A	9965 000 25101	Logic-Buffer(E)
LJ92-00896A	9965 000 25102	Logic-Buffer(F)
LJ92-00994A	9965 000 25103	Y-Buffer(up)
LJ92-00993A	9965 000 25104	Y-Buffer(down)
LJ92-00990E	9965 000 25105	Logic-Board
LJ92-00980A	9965 000 25106	X-Board
LJ92-00981A	9965 000 25107	Y-Board
LJ44-00058A	9965 000 25108	SMPS(PSU)
LJ44-00075A	9965 000 25131	SUB PSU

50"HDv3

PDP type

S50HW-XD03	9322 215 26682	PDP model name (non spare)
S50HW-XB02	9966 000 26017	PDP without PSU

BOARDS

LJ92-00917A	9965 000 25117	Logic-Buffer(E)
LJ92-00918A	9965 000 25118	Logic-Buffer(F)
LJ92-00919A	9965 000 25119	Logic-Buffer(G)
LJ92-00920A	9965 000 25120	Logic-Buffer(H)
LJ92-00921A	9965 000 25121	Logic-Buffer(I)
LJ92-00922A	9965 000 25122	Logic-Buffer(J)
LJ92-00880A	9965 000 25123	Y-Buffer(up)
LJ92-00881A	9965 000 25124	Y-Buffer(down)
LJ92-00949C	9965 000 25125	Logic-Board
LJ92-00923A	9965 000 25126	SUBL
LJ92-00959A	9965 000 25127	SUBR
LJ92-00852A	9965 000 25128	X-Board
LJ92-00853A	9965 000 25129	Y-Board
LJ44-00065A	9965 000 25130	SMPS(PSU)
LJ44-00099A	9965 000 26195	SUB PSU